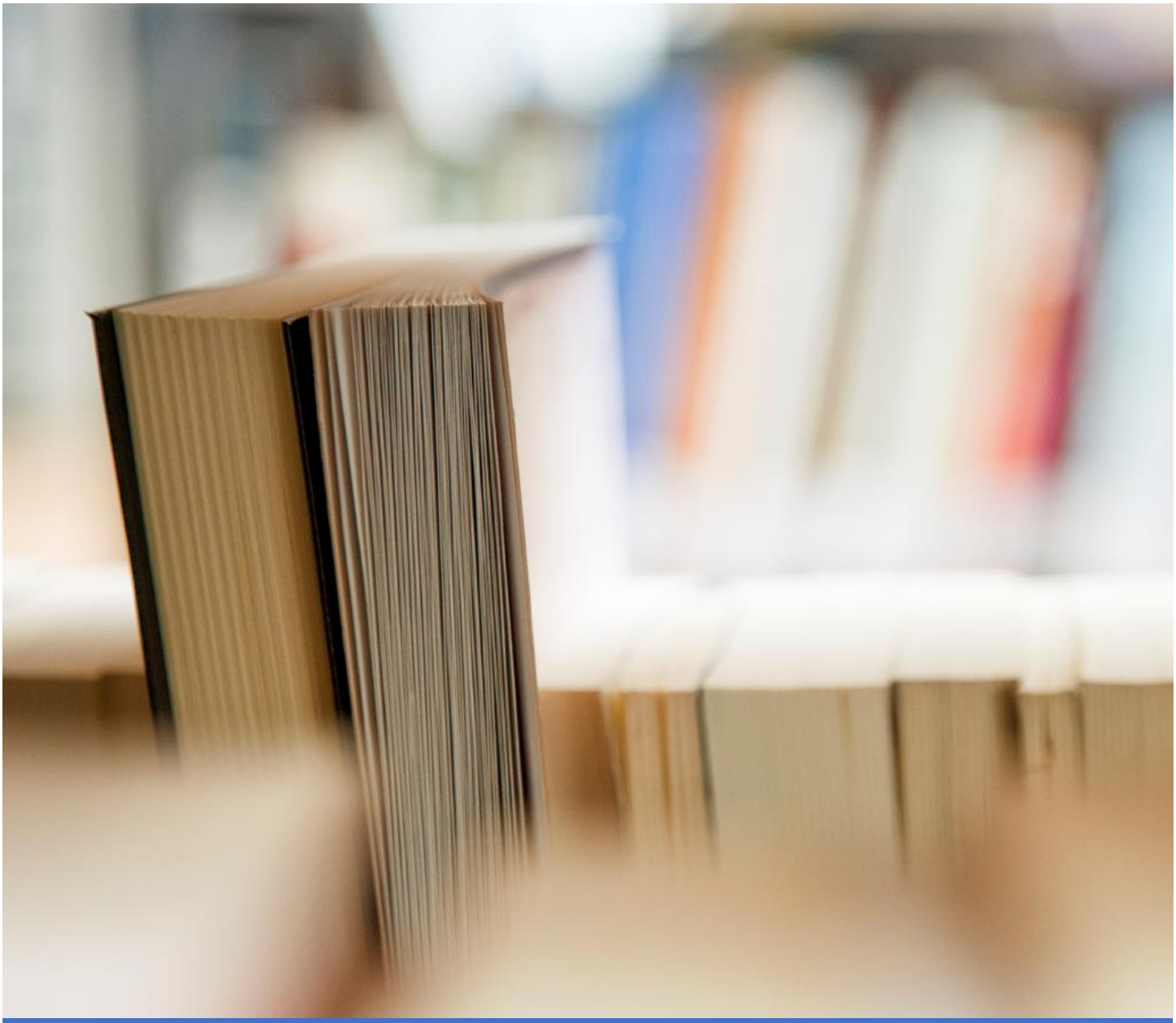


Electronic Second Stage

M.Sc. Zahraa Niema Kamal

Lecture Eight

First Course

Lecture Eight

Clampers

1. Introduction

The clamping network is one that will clamp a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non conducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five-time constants (5τ). The network of Fig. (29) will clamp the input signal to the zero level (for ideal diodes).

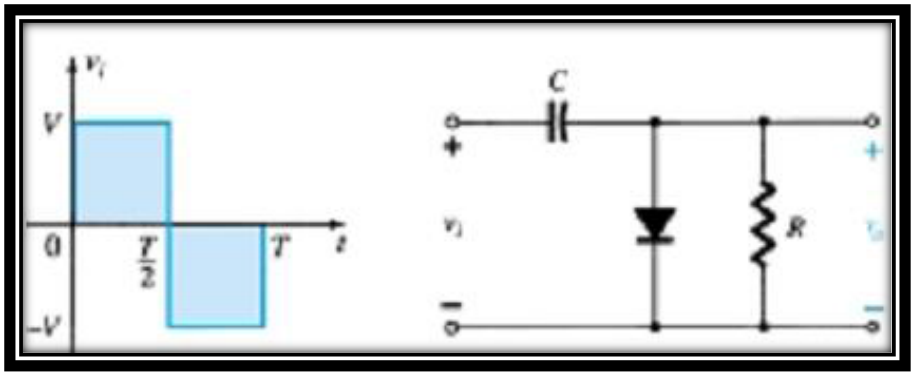


Figure (29) Clamper

During the interval 0 → T/2:

The network will appear as shown in Fig. (30), with the diode in the "**ON**" state effectively "shorting out" the effect of the resistor R. The resulting RC time constant is so small (R determined by the inherent resistance of the network) that the capacitor will charge to V volts very quickly. During this interval the output voltage is directly across the short circuit and **vo = 0v**

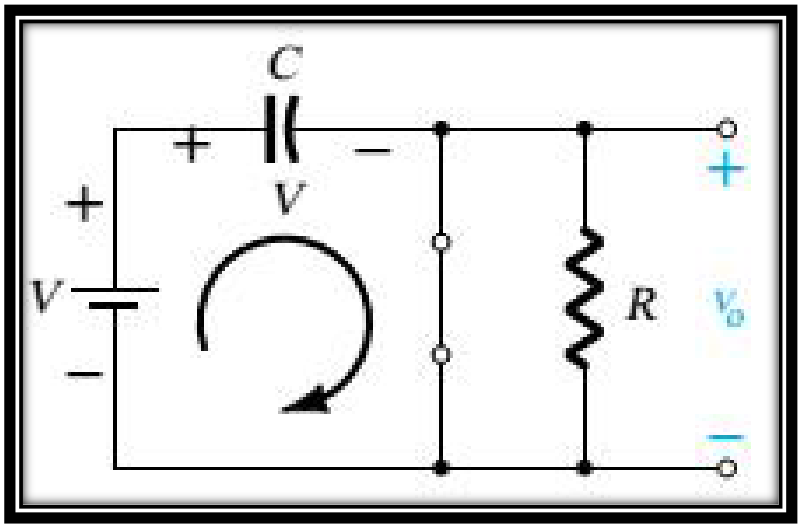


Figure (30) Diode "ON" and the capacitor charging to V volts.

During the interval T/2 → T:

When the input switches to the -V state, the network will appear as shown in Fig. (31), with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the

RC product is sufficiently large to establish a discharge period 5τ much greater than the period T/2 → T, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since **V Q/C**) during this period**.**

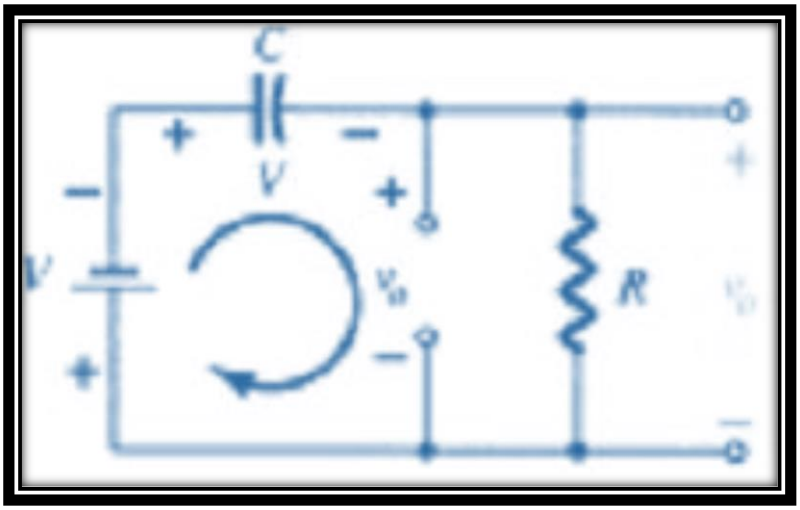


Figure (31) Determining vo with the diode "OFF"

-V-V-vo= 0

Vo=-2V

The resulting output waveform appears in Fig. (32) with the input signal. The output signal is clamped to 0 V for the interval 0 to T/2 but maintains the same total swing (2V) as the input.

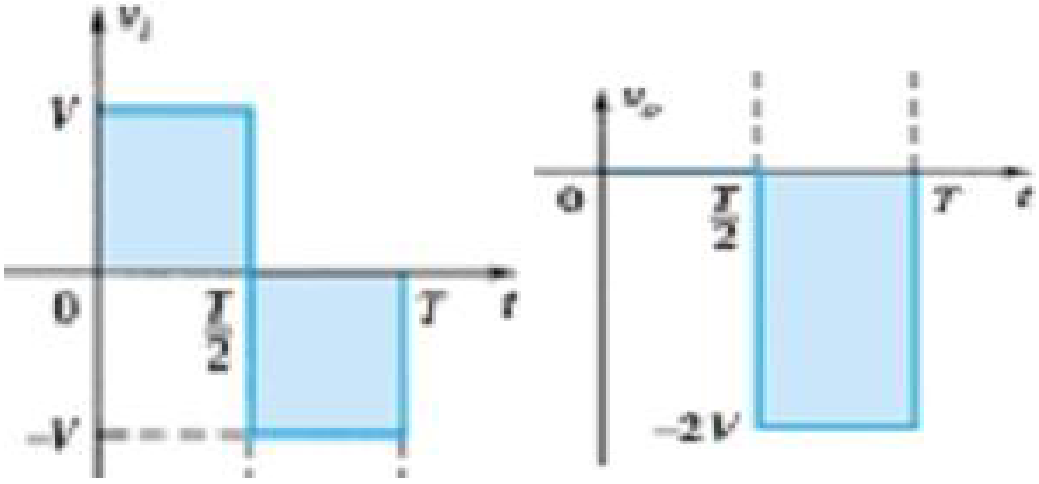


Figure (32) Sketching of vo

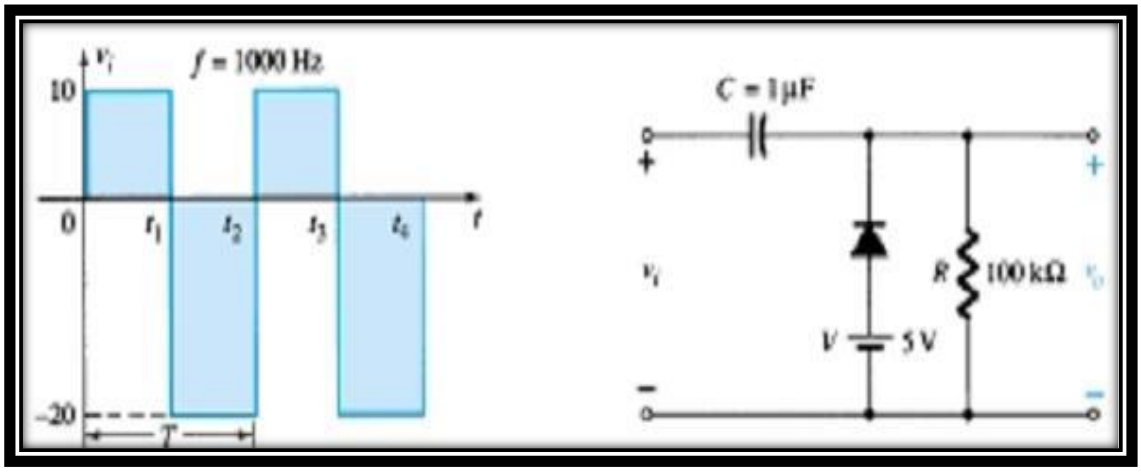
The total swing of the output is equal to the total swing of the input signal.

In general, the following steps may be helpful when analyzing clamping networks:

1. Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.
2. During the period that the diode is in the **ON** state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.
3. Assume that during the period when the diode is in the **OFF** state the capacitor will hold on to its established voltage level.
4. Throughout the analysis maintain a continual awareness of the location and reference polarity for ***vo*** to ensure that the proper levels for ***vo*** are obtained.
5. Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.

Example 1

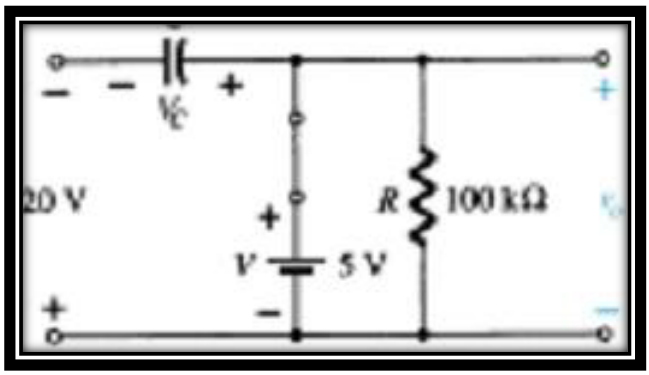
Determine ***vo*** for the network of Fig. below for the input



Solution:

Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.

So, we will start from interval (T1-T2), and find ***vc***:

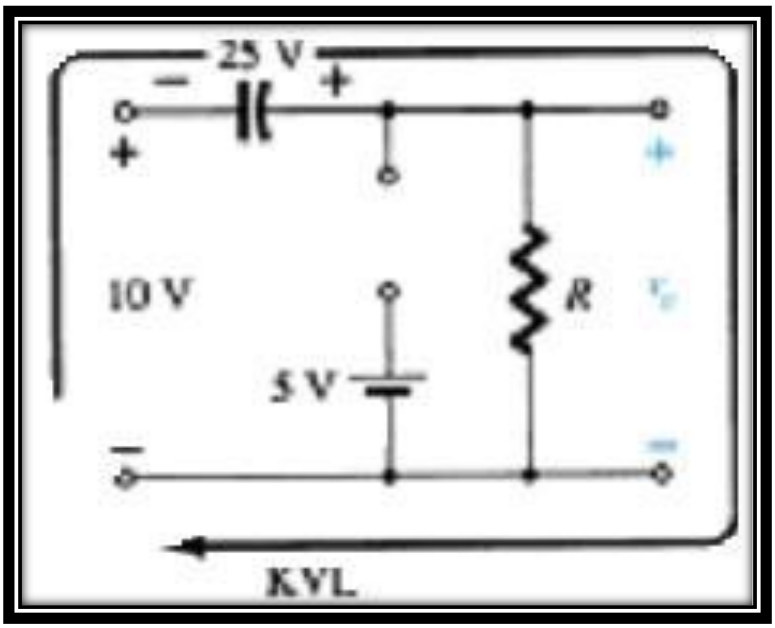


During the period that the diode is in the **ON** state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.

-20V+Vc-5V=0

Vc= 25V

Assume that during the period when the diode is in the **OFF** state the capacitor will hold on to its established voltage level.



$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

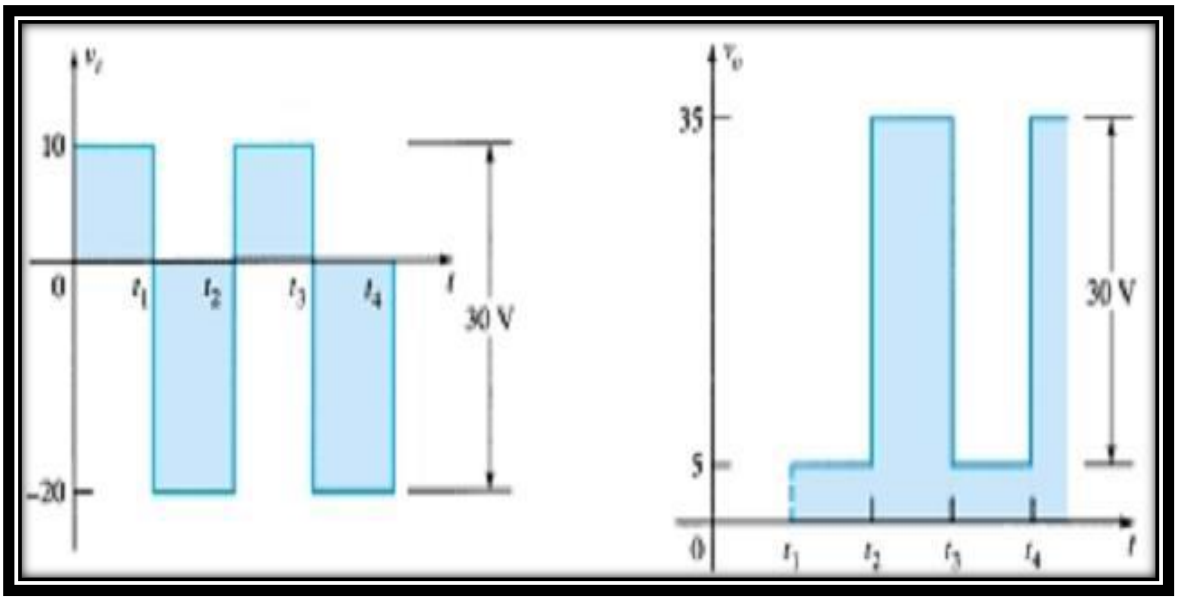
The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Throughout the analysis maintain a continual awareness of the location and reference polarity for ***vo*** to ensure that the proper levels for ***vo*** are obtained.

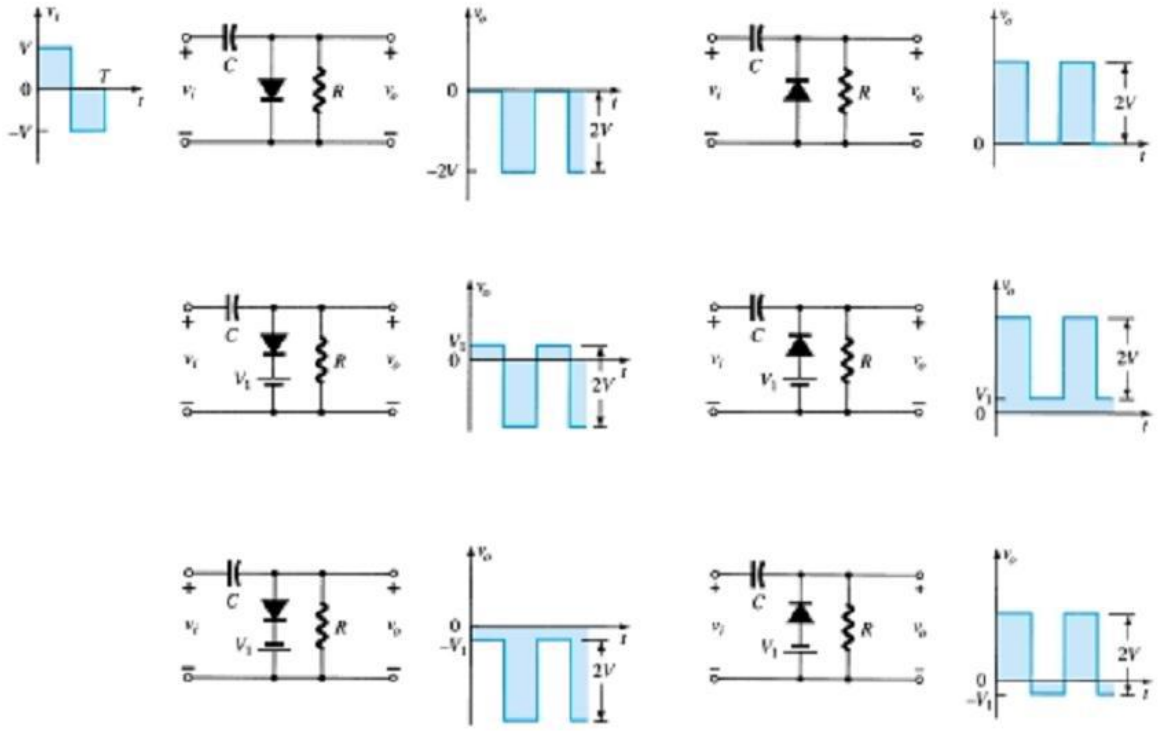
+10V+25V-vo=0

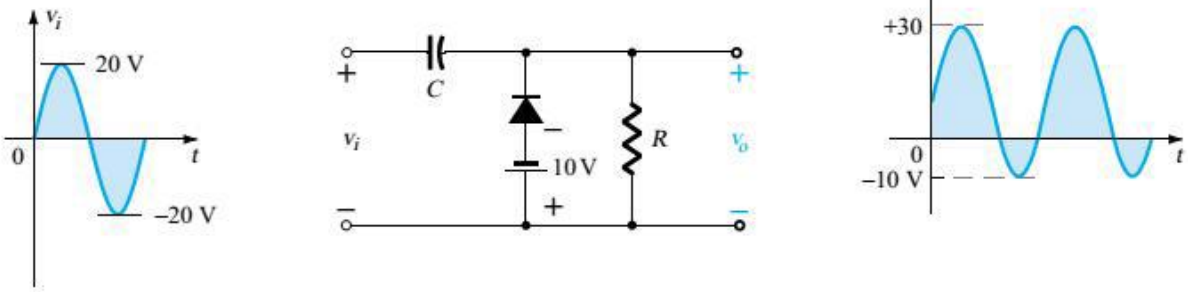
Vo=35V

Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.



H.W: Repeat the example above using **silicon diode** with $\mathbf{V_T = 0.7\ V}$


C
R
2V
V_1


v_i
20 V
0
t
–20 V
C
10 V
R
v_o
v_o (V)
+30
0
–10 V