LECTURE 5

INSTRUCTION SET OF 8085 MICROPROCESSOR

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LOGIC INSTRUCTIONS:

Logical instructions are the instructions which perform basic logical operations such as AND, OR, etc. In 8085 microprocessor, the destination operand is always the accumulator. Here logical operation works on a bitwise level. Following is the table showing the list of logical instructions:

OPCODE	***DESCRIPTION***
ANA	The contents of the accumulator are logically ANDed with the contents of the operand (register or memory), and the result is placed in the accumulator. If the operand is a memory location, its address is specified by the contents of HL registers. S, Z, P are modified to reflect the result of the operation. CY is reset. AC is set. Example: ANA B or ANA M
ANI	The contents of the accumulator are logically ANDed with the 8-bit data (operand) and the result is placed in the accumulator. S, Z, P are modified to reflect the result of the operation. CY is reset. AC is set. Example: ANI 86H
CMP	The contents of the operand (register or memory) are compared with the contents of the accumulator. Both contents are preserved.

The result of the comparison is shown by setting the flags of the PSW as follows:
if (A) < (reg/mem): carry flag is set
if (A) = (reg/mem): zero flag is set
if (A) > (reg/mem): carry and zero flags are reset
Example: CMP B or CMP M

CPI

The second byte (8-bit data) is compared with the contents of the accumulator. The values being compared remain unchanged. The result of the comparison is shown by setting
the flags of the PSW as follows:
if (A) < data: carry flag is set
if (A) = data: zero flag is set
if (A) > data: carry and zero flags are reset
Example: CPI 89H

XRA

The contents of the accumulator are Exclusive ORed with the contents of the operand (register or memory), and the result is placed in the accumulator. If the operand is a memory location, its address is specified by the contents of HL registers. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.
Example: XRA B or XRA M

XRI

The contents of the accumulator are Exclusive ORed with the 8-bit data (operand) and the result is placed in the accumulator. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.

Example: XRI 86H

ORA

The contents of the accumulator are logically ORed with the contents of the operand (register or memory), and the result is placed in the accumulator. If the operand is a memory location, its address is specified by the contents of HL registers. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.
Example: ORA B or ORA M

ORI

The contents of the accumulator are logically ORed with the 8-bit data (operand) and the result is placed in the accumulator. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.
Example: ORI 86H

CMA

The contents of the accumulator are complemented.

CMC

The Carry flag is complemented.

STC

The Carry flag is set to 1.

BRANCH INSTRUCTION:

Branching instructions refer to the act of switching execution to a different instruction sequence as a result of executing a branch instruction.

Jump Instructions

The jump instruction transfers the program sequence to the memory address given in the operand based on the specified flag. Jump instructions are 2 types: Unconditional Jump Instructions and Conditional Jump Instructions.

JMP (Unconditional) Jump)		The program sequence is transferred to the memory location specified by the 16-bit address given in the operand. Example: JMP 2034H or JMP XYZ
JC	(Conditional Jump)	Jump on Carry CY = 1
JNC		Jump on no Carry CY = 0
JM		Jump on minus S = 1
JZ		Jump on zero Z = 1
JNZ		Jump on no zero Z = 0
JPE		Jump on parity even P = 1
JPO		Jump on parity odd P = 0
PCHL		The contents of registers H and L are copied into the program counter. The contents of H are placed as the high-order byte and the contents of L as the low-order byte. Example: PCHL

CONTROL INSTRUCTION:

These type of instructions control machine functions such as Halt, Interrupt, or do nothing. This type of instructions alters the different type of operations executed in the processor.

NOP

No operation is performed. The instruction is fetched decoded. However no operation is executed.
Example: NOP

HLT

The CPU finishes executing the current instruction and halts any further execution. An interrupt or reset is necessary to exit from the halt state.
Example: HLT

RIM

This is a multipurpose instruction used to read the status of interrupts 7.5, 6.5, 5.5 and read serial data input bit. The instruction loads eight bits in the accumulator with the following interpretations.
Example: RIM

SIM

This is a multipurpose instruction and used to implement the 8085 interrupts 7.5, 6.5, 5.5, and serial data output. The instruction interprets the accumulator contents as follows.
Example: SIM