Al-Mustaqbal University Collage
Department Of Computer Engineering Techniques
M.Sc. Hasan Muwafaq Gheni

LECTURE FOUR

Interfacing The 8085 Microprocessor

(I/O & Memory Interfacing)

BY:

M.Sc.: HASAN MUWAFAQ GHENI

The memory interfacing requires to:

- **Select the chip**
- **Identify the register**
- **Enable the appropriate buffer.**

Microprocessor system includes memory devices and I/O devices. It is important to note that microprocessor can communicate (read/write) with only one device at a time, since the data, address and control buses are common for all the devices. In order to communicate with memory or I/O devices, it is necessary to decode the address from the microprocessor. Due to this each device (memory or I/O) can be accessed independently. The following section describes common address decoding techniques.

Al-Mustaqbal University Collage
Department Of Computer Engineering Techniques
M.Sc. Hasan Muwafaq Gheni

Address Decoding Techniques:

- **Absolute decoding/Full Decoding**
- **Linear decoding/Partial Decoding**

Absolute decoding:

In absolute decoding technique, all the higher address lines are decoded to select the memory chip, and the memory chip is selected only for the specified logic levels on these high-order address lines; no other logic levels can select the chip.

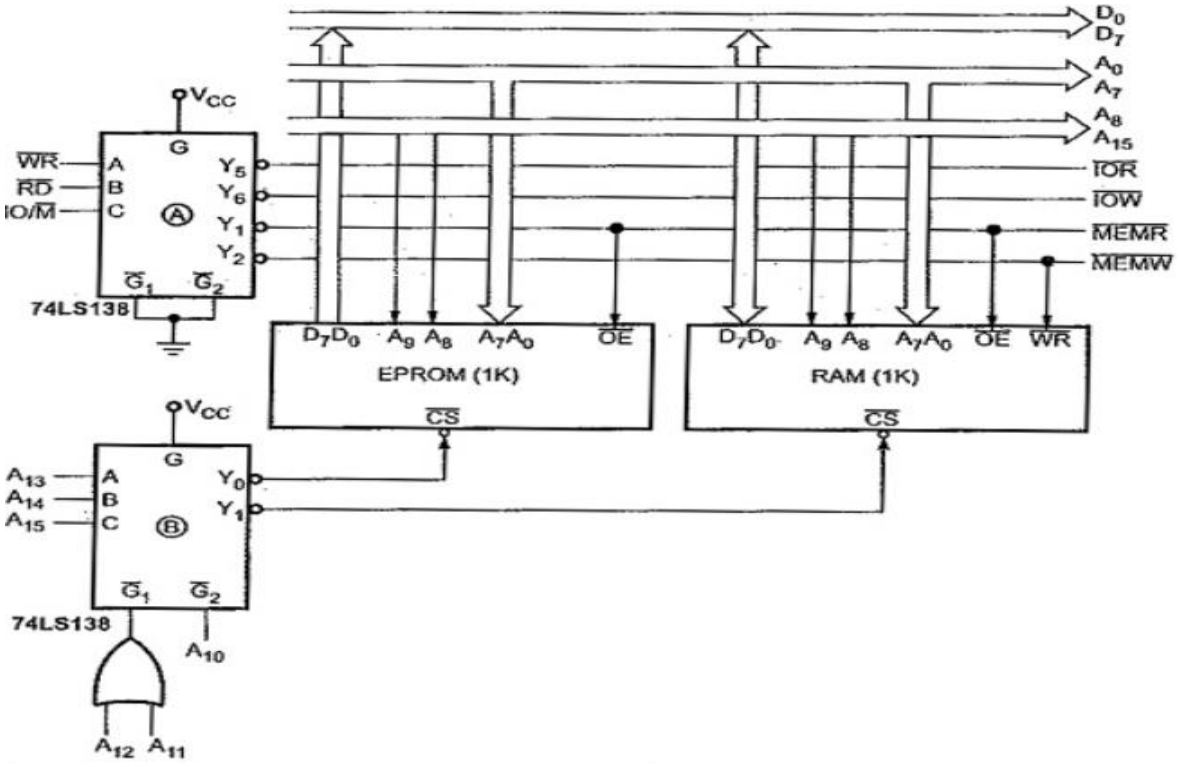

Figure shows the Memory Interfacing in 8085 with absolute decoding. This addressing technique is normally used in large memory systems.

Linear decoding:

In small systems, hardware for the decoding logic can be eliminated by using individual high-order address lines to select memory chips. This is referred to as linear decoding. Figure shows the addressing of RAM with linear decoding technique. This technique is also called **partial decoding**. It reduces the cost of decoding circuit, but it has a drawback of multiple addresses (shadow addresses).

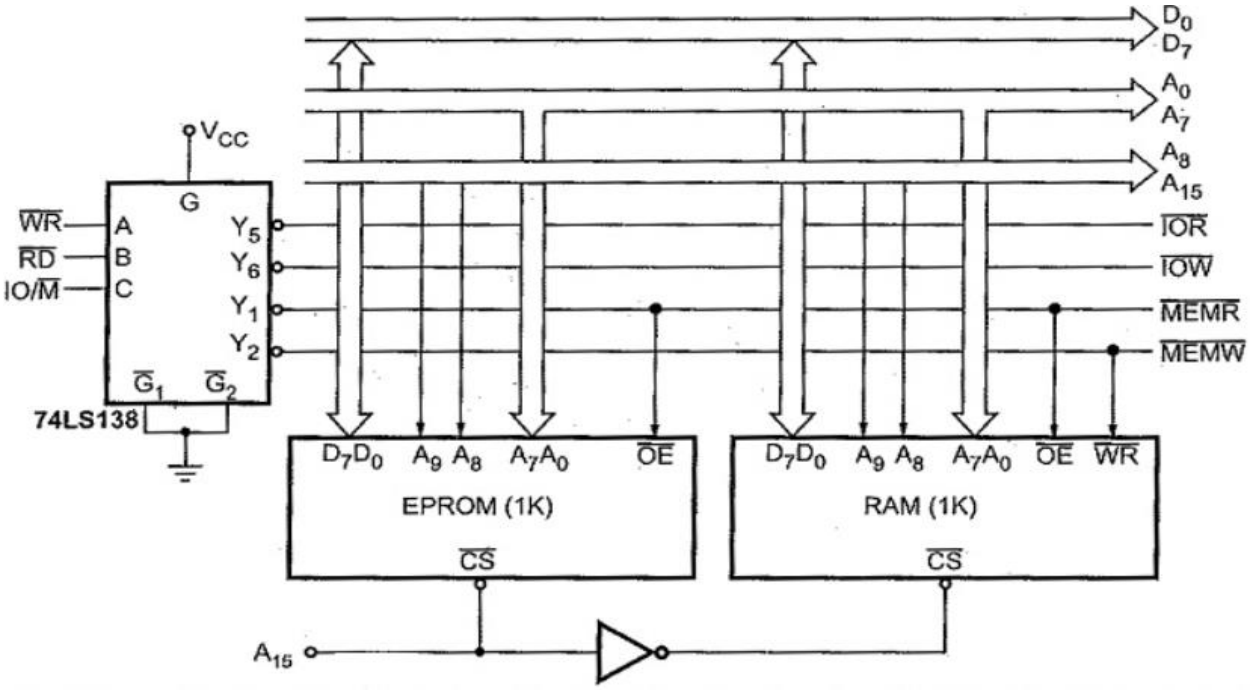

Figure shows the addressing of RAM with linear decoding technique. A_{15} address line, is directly connected to the chip select signal of EPROM and after inversion it is connected to the chip select signal of the RAM. Therefore, when the status of A_{15} line is ‘zero’, EPROM gets selected and when the status of A_{15} line is ‘one’ RAM gets selected. The status of the other address lines is not considered, since those address lines are not used for generation of chip select signals.