

MOSFET

ENHANCEMENT-TYPE MOSFET:

- 1-p -type material is formed from a silicon base and is again referred to as the substrate
- 2-the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.
- 3-The drain current is now cut off until the gate-to-source voltage reaches a specific magnitude

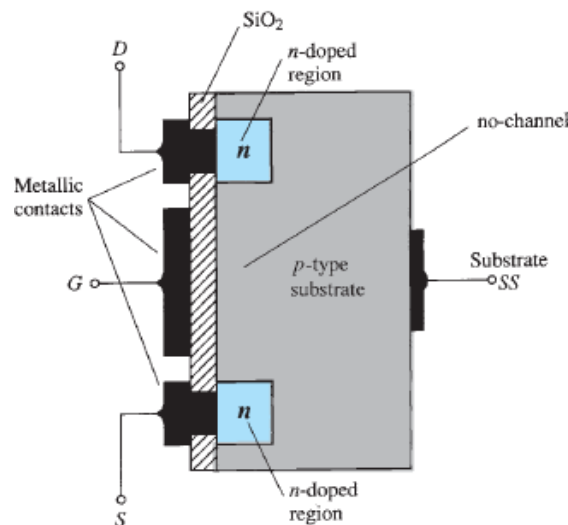


FIG. 6.32
n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics:

- 1- If V_{GS} is set at 0V and a voltage applied between the drain and the source of the device of Fig. 6.32, the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0A

2-In Fig.6.33, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0V, establishing the drain and the gate at a positive potential with respect to the source

3-The positiv potential at the gate will pressure the holes (since like charges repel) in the p -substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p -substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the p -substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer.

4- with V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced n -type region can support a measurable flow between drain and source

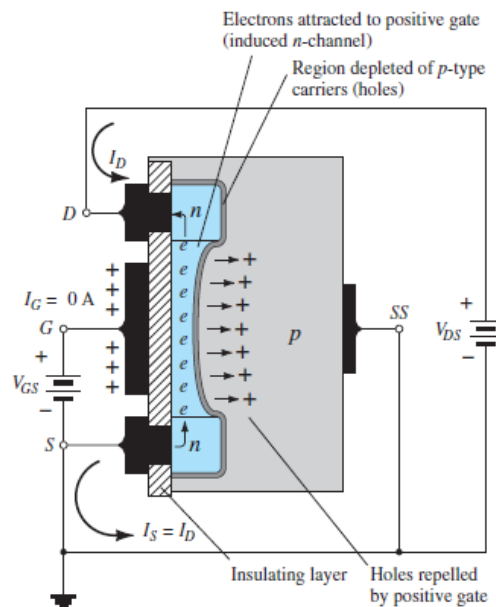


FIG. 6.33
Channel formation in the n-channel enhancement-type MOSFET.

The level of V_{GS} that results in the significant increase in drain current is called the **threshold voltage** and is given the symbol V_T . As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS} , the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 6.34. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 6.34, we find that

$$V_{DG} = V_{DS} - V_{GS} \quad (6.13)$$

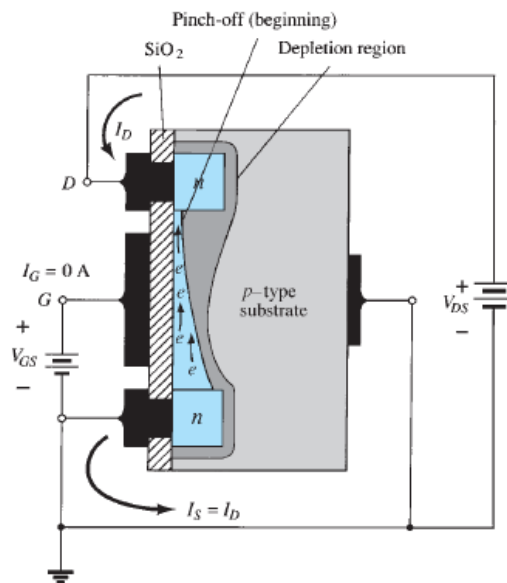


FIG. 6.34
 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS} .

The drain characteristics of Fig. 6.35 reveal that for the device of Fig. 6.34 with $V_{GS} = 8\text{ V}$, saturation occurs at a level of $V_{DS} = 6\text{ V}$. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DS_{sat}} = V_{GS} - V_T \quad (6.14)$$



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Lecture: 10- MOSFET

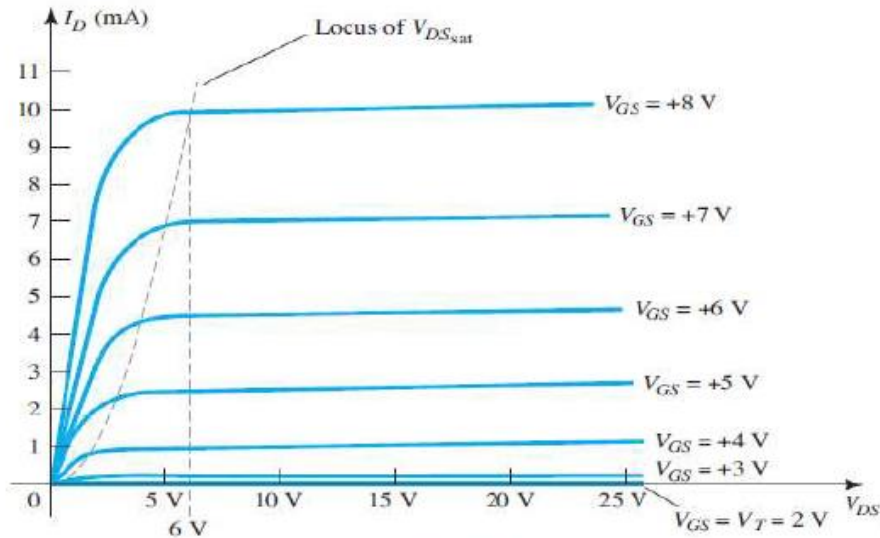


FIG. 6.35

Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2\text{ V}$ and $k = 0.278 \times 10^{-3}\text{ A/V}^2$.

For values of V_{GS} less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2 \quad (6.15)$$

V_{GS} . The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (6.15)], where $I_{D(\text{on})}$ and $V_{GS(\text{on})}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2} \quad (6.16)$$

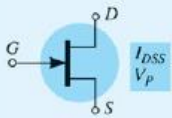
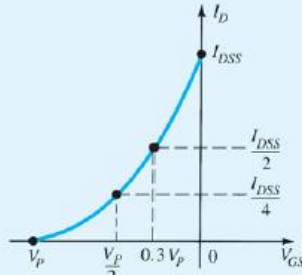
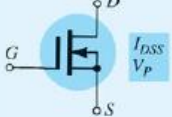
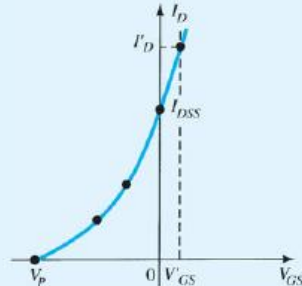
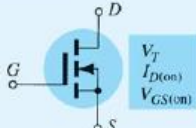
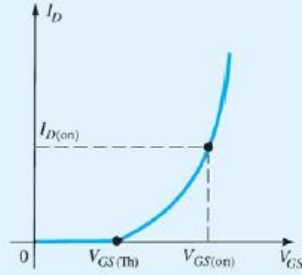
Substituting $I_{D(\text{on})} = 10\text{ mA}$ when $V_{GS(\text{on})} = 8\text{ V}$ from the characteristics of Fig. 6.35 yields

$$\begin{aligned} k &= \frac{10\text{ mA}}{(8\text{ V} - 2\text{ V})^2} = \frac{10\text{ mA}}{(6\text{ V})^2} = \frac{10\text{ mA}}{36\text{ V}^2} \\ &= 0.278 \times 10^{-3}\text{ A/V}^2 \end{aligned}$$

SUMMARY:

1. A current-controlled device is one in which a current defines the operating conditions of the device, whereas a voltage-controlled device is one in which a particular voltage defines the operating conditions.
2. The JFET can actually be used as a voltage-controlled resistor because of a unique sensitivity of the drain-to-source impedance to the gate-to-source voltage.
3. The maximum current for any JFET is labeled I_{DSS} and occurs when $V_{GS} = 0$ V.
4. The minimum current for a JFET occurs at pinch-off defined by $V_{GS} = V_P$.
5. The relationship between the drain current and the gate-to-source voltage of a JFET is a nonlinear one defined by Shockley's equation. As the current level approaches I_{DSS} , the sensitivity of I_D to changes in V_{GS} increases significantly.

TABLE 6.3
Field Effect Transistors

Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (n-channel)	$I_G = 0$ A, $I_D = I_S$  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100$ M Ω $C_i: (1 - 10)$ pF
MOSFET depletion type (n-channel)	$I_G = 0$ A, $I_D = I_S$  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10}$ Ω $C_i: (1 - 10)$ pF
MOSFET enhancement type (n-channel)	$I_G = 0$ A, $I_D = I_S$  $I_D = k (V_{GS} - V_{GS(th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$		$R_i > 10^{10}$ Ω $C_i: (1 - 10)$ pF

FET BIASING

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0 \text{ A} \quad (7.1)$$

and

$$I_D = I_S \quad (7.2)$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad (7.3)$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \quad (7.4)$$

FIXED-BIAS CONFIGURATION:

The coupling capacitors are "open circuits" for the dc analysis

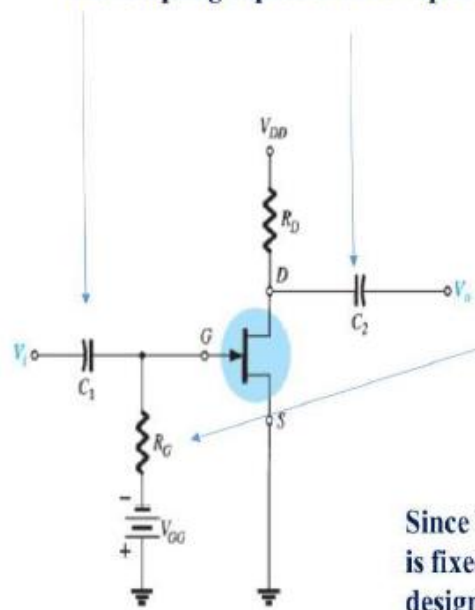


FIG. 7.1
Fixed-bias configuration.

For the dc analysis,

$$I_G \cong 0 \text{ A}$$

$$V_{R_G} = I_G R_G = (0 \text{ A}) R_G = 0 \text{ V}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

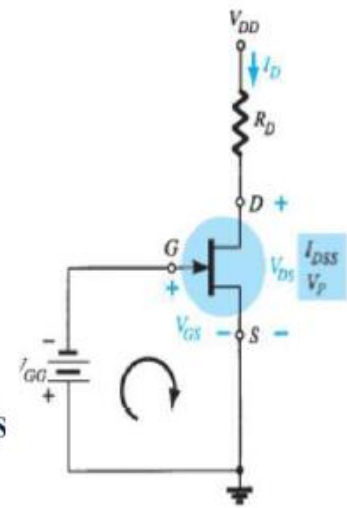
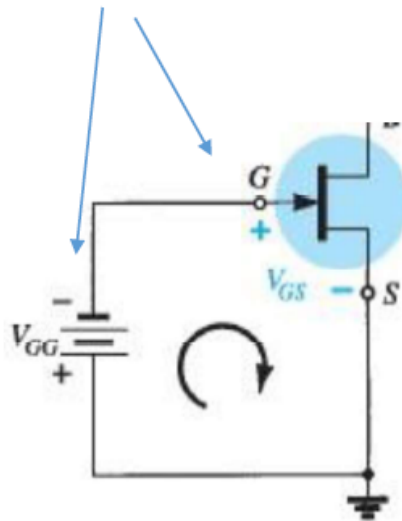


FIG. 7.2
Network for dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG} .



Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 7.2 results in

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$-V_{GG} - V_{GS} = 0$$

$V_{GS} = -V_{GG}$

The intersection just described will be sufficient for plotting the curve

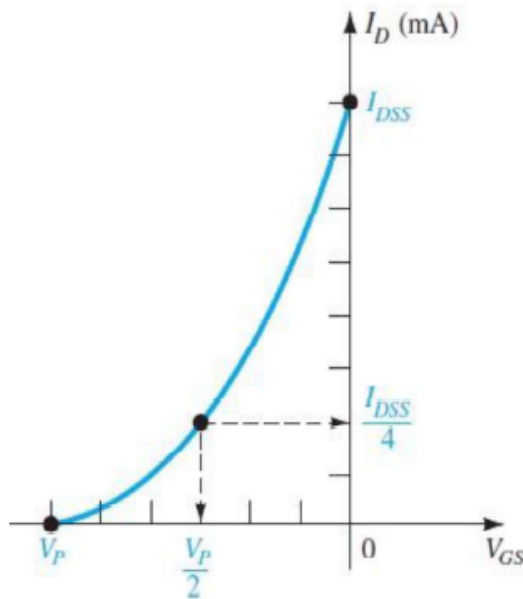


FIG. 7.3

Plotting Shockley's equation.

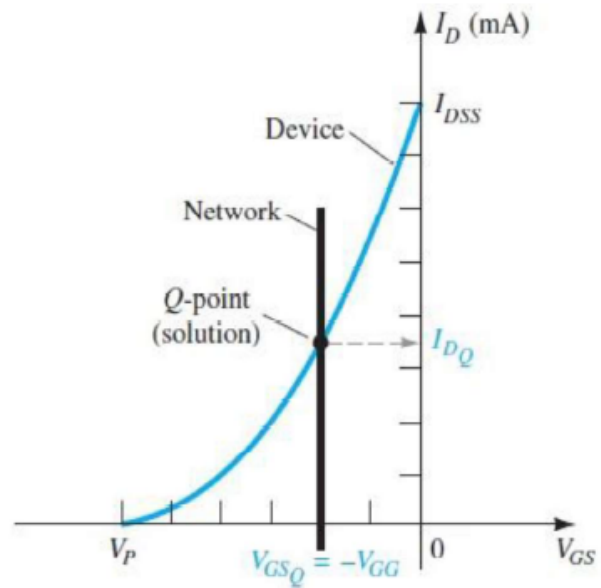
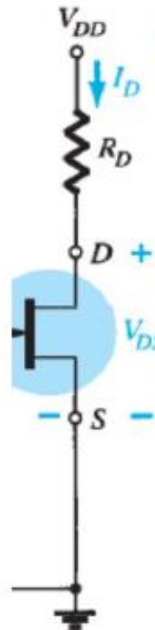


FIG. 7.4

Finding the solution for the fixed-bias configuration.



The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - I_D R_D$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 7.2 ,

$$V_S = 0 \text{ V}$$

or

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S = V_{DS} + 0 \text{ V}$$

and

$$V_D = V_{DS}$$

In addition,

$$V_{GS} = V_G - V_S$$

$$V_G = V_{GS} + V_S = V_{GS} + 0 \text{ V}$$

or

and

$$V_G = V_{GS}$$

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

- a. V_{GSQ}
- b. I_{DQ}
- c. V_{DS}
- d. V_D
- e. V_G
- f. V_S

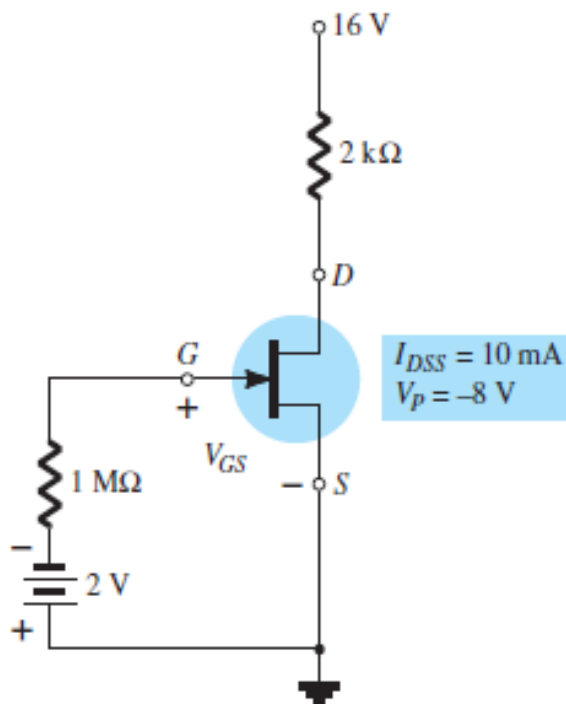


FIG. 7.6
 Example 7.1.

Solution:

Mathematical Approach

- a. $V_{GSQ} = -V_{GG} = -2 \text{ V}$
- b.
$$I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 = 10 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-8 \text{ V}} \right)^2$$

$$= 10 \text{ mA} (1 - 0.25)^2 = 10 \text{ mA} (0.75)^2 = 10 \text{ mA} (0.5625)$$

$$= 5.625 \text{ mA}$$
- c.
$$V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.625 \text{ mA})(2 \text{ k}\Omega)$$

$$= 16 \text{ V} - 11.25 \text{ V} = 4.75 \text{ V}$$
- d. $V_D = V_{DS} = 4.75 \text{ V}$
- e. $V_G = V_{GS} = -2 \text{ V}$
- f. $V_S = 0 \text{ V}$