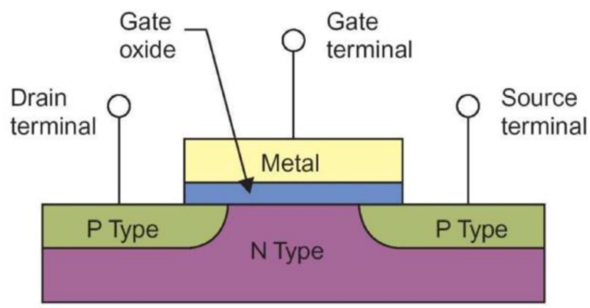
Al-Mustaqbal University
College of Engineering and Technologies
Medical Instrumentation Technique Engineering Department
Class: 2nd
Subject: Electronic Circuits
Lecturer: Dr. Rami Qays Malik
Lecture: 9- Field Effect Transistor 1

Field Effect Transistor (FET)



1. INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow. The primary difference between the two types of transistors is the fact that: The BJT transistor is a current-controlled device as depicted in Fig. 6.1, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.

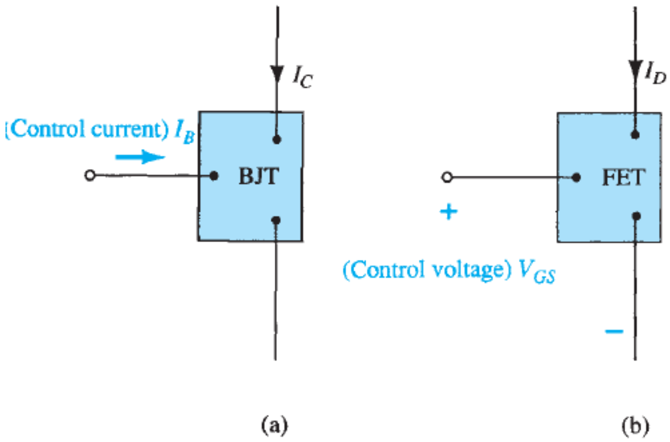


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

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BJT	FET
current-controlled device	**voltage-controlled device**
bipolar device	**unipolar device**
Lower Input impedance Compered with FET	high input impedance
Higher sensitivity to changes in the applied signal.	Low sensitivity to changes in the applied signal.
Less Temperature stable	more temperature stable
Larger in construction	smaller in construction

2. CONSTRUCTION AND CHARACTERISTICS OF JFETs

1-the JFET (junction field-effect transistor) is a three-terminal device with one terminal capable of controlling the current between the other two

2-the major part of the structure is the n -type material, which forms the channel between the embedded layers of p -type material

3-the drain and the source are connected to the ends of the n -type channel and the gate to the two layers of p -type material

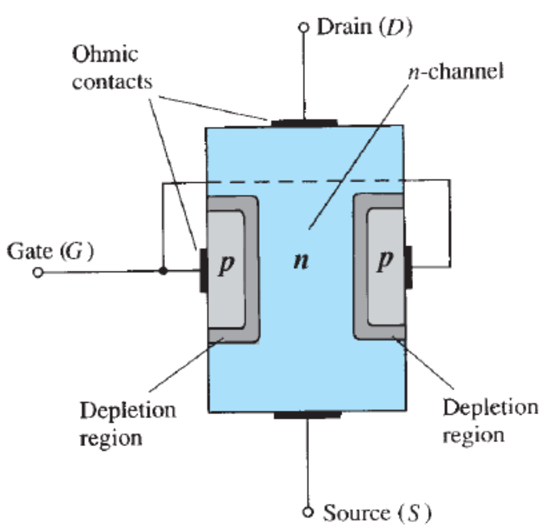

FIG. 6.3
Junction field-effect transistor (JFET).

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for the JFET transistor can defined the following

1-The input circuit (gate to source) of a Jfet is reverse bias, that means the device has high input impedance

2-the drain is so biased with respect to the source , ID flows from source to drain

3- in all Jfet ID=IS

When

V_{GS} = 0 V, VDS Some Positive Value

- a positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition V_{GS} = 0 V.

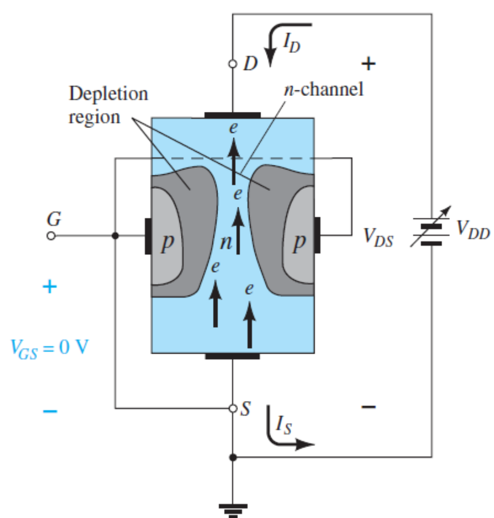

FIG. 6.5
JFET at V_{GS} = 0 V and V_{DS} > 0 V.

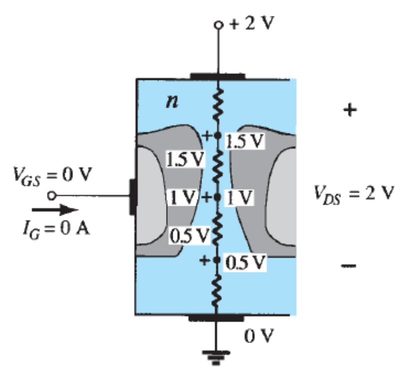

FIG. 6.6
Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

The current ID will establish the voltage levels through the channel the greater the applied reverse bias in p type material , the wider is the depletion region.

I_D versus V_{DS} for V_{GS} = 0 V.

At first I_D rises rapidly with V_{DS} but then becomes constant The V_{DS} above which I_D becomes constant is known as pinch of voltage After pinched of the channel width becomes so narrow that depletion layers almost touch each other and I_D maintains a saturation level defined as I_{DSS} with a current of very high density.

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Pinch-off (V_{GS} = 0 V, V_{DS} = V_P).

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions V_{GS} = 0 V and $V_{DS} > V_P$.

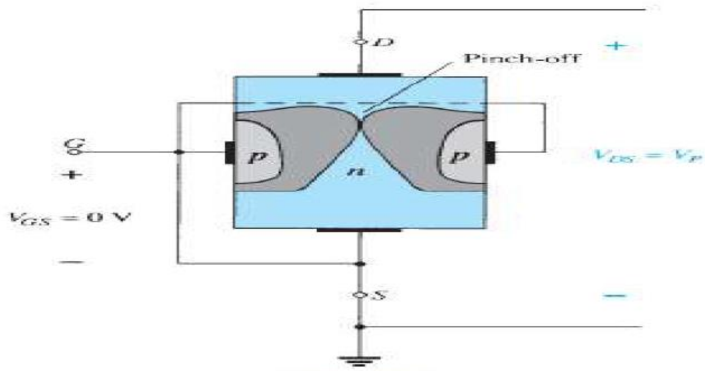

FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

When V_{GS} <0 V

V_{GS} is The voltage from gate to source a negative voltage is applied between G and S

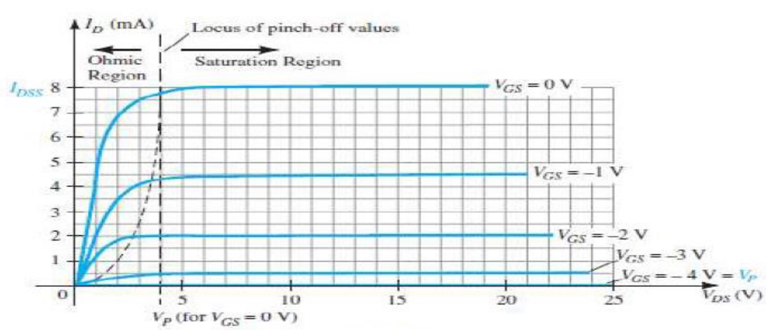

FIG. 6.11
n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

The resulting saturation level for ID has been reduced and in fact will continue to decrease as VGS is made more and more negative and a pinch-off voltage continues to drop as VGS becomes more and more negative and the device has been (Turned Off) In summary:

The level of VGS that results in ID = 0 mA is defined by VGS =VP, with VP being a negative voltage for n channel devices and a positive voltage for p-channel JFETs.

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Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 6.11 is referred to as the ohmic or voltage-controlled resistance region. possibly for an automatic gain control system whose resistance is controlled by the applied gate-to-source voltage

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \qquad \textbf{(6.1)}$$

where r_o is the resistance with $V_{GS} = 0$ V and r_d is the resistance at a particular level of V_{GS}.

For an n-channel JFET with $r_o = 10\ \text{k}\Omega$ ($V_{GS} = 0$ V, $V_P = -6$ V), Eq. (6.1) results in 40 kΩ at $V_{GS} = -3$ V.

p -Channel Devices

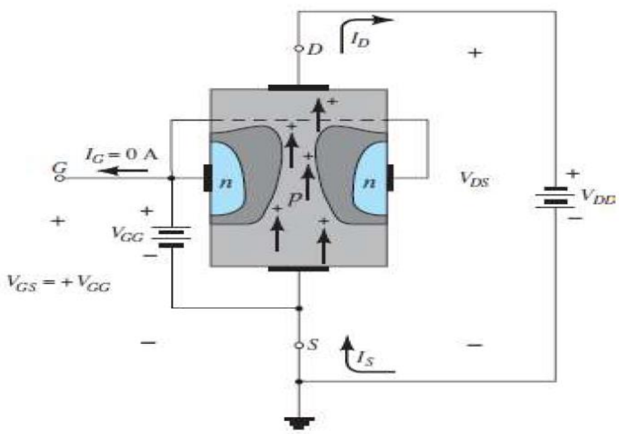

FIG. 6.12
p-Channel JFET.

The defined current directions are reversed Applied voltage is positive voltages from gate to source and the double-subscript notation for VDS will result in negative voltages for VDS

Summary

A- The maximum current is defined as IDSS and occurs when VGS=0 V and VDS ≥ VP ,

B- For gate-to-source voltages VGS is less than (more negative than) the pinch-off level, the drain current is 0 A (ID = 0 A)

C- For all levels of VGS between 0 V and the pinch-off level, the current ID will range between IDSS and 0 A, respectively.

D- A similar list can be developed for p-channel JFETs.

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6.3 TRANSFER CHARACTERISTICS

The relationship between *I D* and *V GS* is defined by *Shockley's equation*

control variable (V_{GS})

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \textbf{(6.3)}$$

constants (I_{DSS}, V_P)

In review:

$$\text{When } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS} \qquad \textbf{(6.4)}$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\text{When } V_{GS} = V_P, \quad I_D = 0\text{ mA} \qquad \textbf{(6.5)}$$

Applying Shockley's Equation

Substituting $V_{GS} = 0$ V gives

$$\text{Eq. (6.3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$I_D = I_{DSS}\big|_{V_{GS}=0\text{ V}} \qquad \textbf{(6.6)}$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$

$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$I_D = 0\text{ A}\big|_{V_{GS}=V_P} \qquad \textbf{(6.7)}$$

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8\text{ mA}\left(1 - \frac{-1\text{ V}}{-4\text{ V}}\right)^2 = 8\text{ mA}\left(1 - \frac{1}{4}\right)^2 = 8\text{ mA}(0.75)^2$$

$$= 8\text{ mA}(0.5625)$$

$$= \mathbf{4.5\text{ mA}}$$

By using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of V_{GS} for a given level of I_D. The derivation is quite straightforward and results in equation (6.8)

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \qquad \textbf{(6.8)}$$

Let us test Eq. (6.8) by finding the level of V_{GS} that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 6.17. We find

$$V_{GS} = -4\text{ V}\left(1 - \sqrt{\frac{4.5\text{ mA}}{8\text{ mA}}}\right)$$

$$= -4\text{ V}(1 - \sqrt{0.5625}) = -4\text{ V}(1 - 0.75)$$

$$= -4\text{ V}(0.25)$$

$$= \mathbf{-1\text{ V}}$$

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Shorthand Method

If we specify V_{GS} to be one-half the pinch-off value V_P, the resulting level of I_D will be the following, as determined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$
$$= I_{DSS}(0.25)$$

and $$I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS}=V_P/2} \qquad (6.9)$$

The result specifies that the drain current will always be one-fourth the saturation level I_{DSS} as long as the gate-to-source voltage is one-half the pinch-off value

If we choose $I_D = I_{DSS}/2$ and substitute into Eq. (6.8), we find that

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$
$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

and $$V_{GS} \cong 0.3V_P\big|_{I_D=I_{DSS}/2} \qquad (6.10)$$

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

Solution: Two plot points are defined by

$$I_{DSS} = 12\text{ mA} \quad \text{and} \quad V_{GS} = 0\text{ V}$$

and $$I_D = 0\text{ mA} \quad \text{and} \quad V_{GS} = V_P$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = -3$ **V** the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = 3$ **mA**. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = 6$ **mA** the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = -1.8$ **V**. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

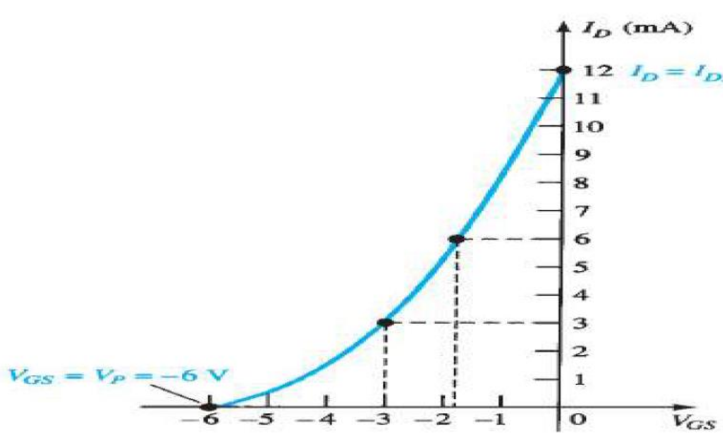

FIG. 6.18
Transfer curve for Example 6.1.

EXAMPLE 6.2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\ V}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\ mA}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\ mA}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\ V}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P.

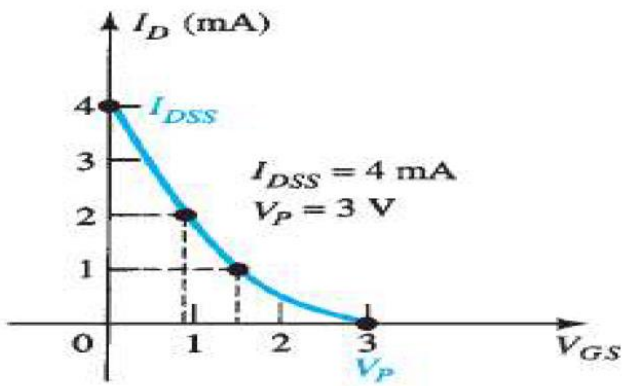

FIG. 6.19
Transfer curve for the p-channel device of Example 6.

6.4 DEPLETION-TYPE MOSFET

As noted in the introduction, there are three types of FETs: JFETs, MOSFETs, and MESFETs. MOSFETs are further broken down into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation; the name MOSFET stands for *m*etal –*o*xide– *s*emiconductor *f*ield -*e*ffect *t*ransistor

Basic Construction

1-A slab of p -type material is formed from a silicon base and is referred to as the substrate.

2- In some cases the substrate is internally connected to the source terminal

3-The source and drain terminals are connected through metallic contacts to n -doped regions linked by an n -channel as shown in the figure

4-The gate is also connected to a metal contact surface but remains insulated from the n -channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a type of insulator referred to as a dielectric

There is no direct electrical connection between the gate terminal and the channel of a MOSFET
It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

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Basic Operation and Characteristics

In Fig. 6.25 the gate-to-source voltage is set to 0 V ،The result is a current similar to that flowing in the channel of the JFET، In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}

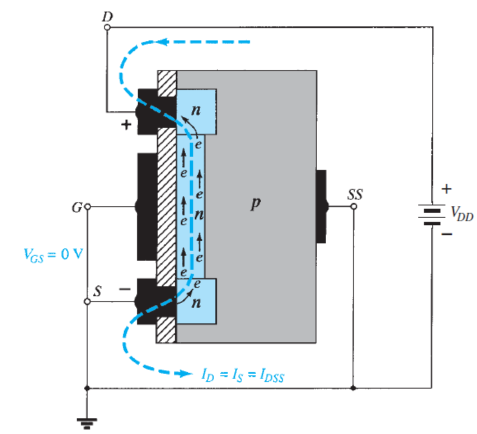

FIG. 6.25
n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.

In Fig. 6.27, VGS is set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p -type substrate (like charges repel) and attract holes from the p -type substrate (opposite charges attract) as shown in Fig. 6.27. Depending on the magnitude of the negative bias established by VGS, The resulting level of drain current is therefore reduced with increasing negative bias for VGS

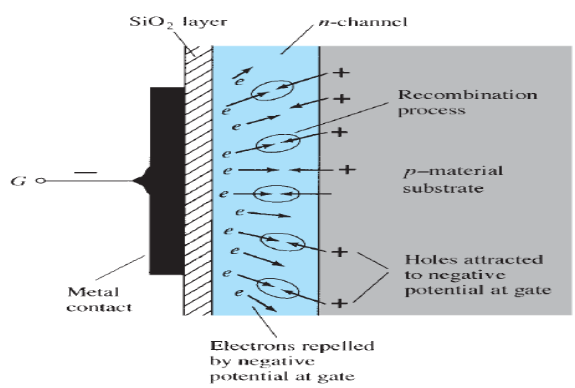

FIG. 6.27
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

EXAMPLE 6.3 Sketch the transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Solution:

$$\text{At } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS} = 10\text{ mA}$$
$$V_{GS} = V_P = -4\text{ V}, \quad I_D = 0\text{ mA}$$
$$V_{GS} = \frac{V_P}{2} = \frac{-4\text{ V}}{2} = -2\text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10\text{ mA}}{4} = 2.5\text{ mA}$$

and at $I_D = \dfrac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$$

all of which appear in Fig. 6.28.

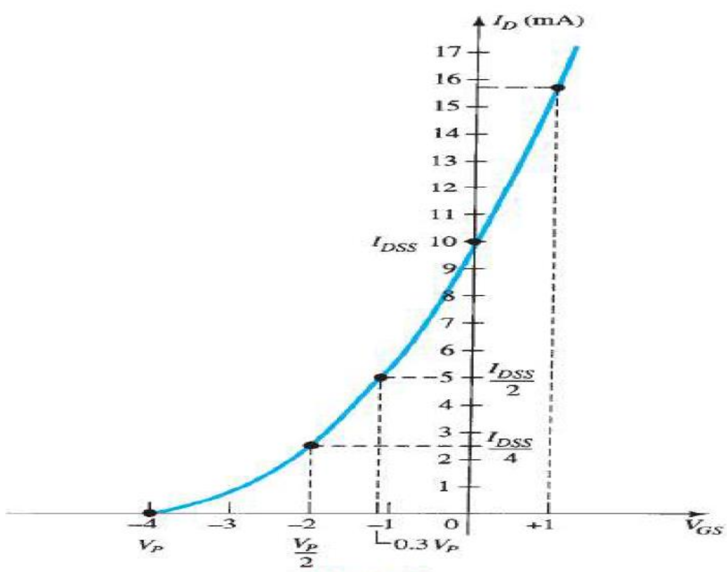

FIG. 6.28
Transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= (10\text{ mA})\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = (10\text{ mA})(1 + 0.25)^2 = (10\text{ mA})(1.5625)$$
$$\cong 15.63\text{ mA}$$

which is sufficiently high to finish the plot.