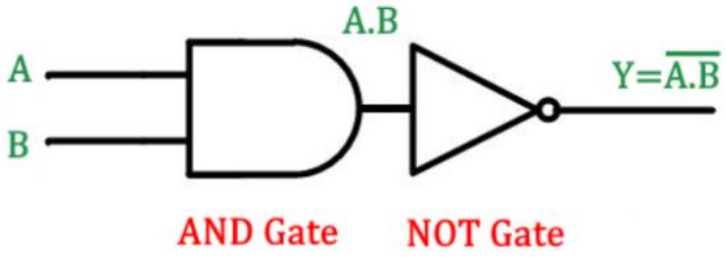
Logic Gate

Digital Electronics Laboratory
Lecturer: Dr Samir Badrawi
Eng. Noor Adnan Madlool

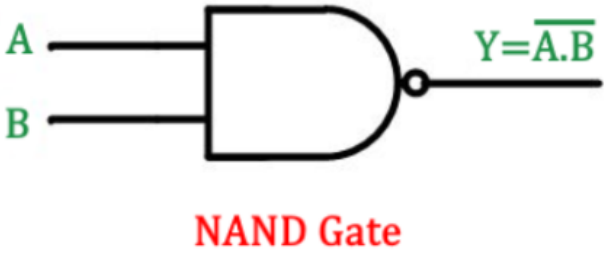
SB@20240329

Lab. Works : Experiment 4: Play with Logic Gates



A	B	A.B	$Y = \overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

=



Truth table

A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

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(a) : NOT gate from NAND gates

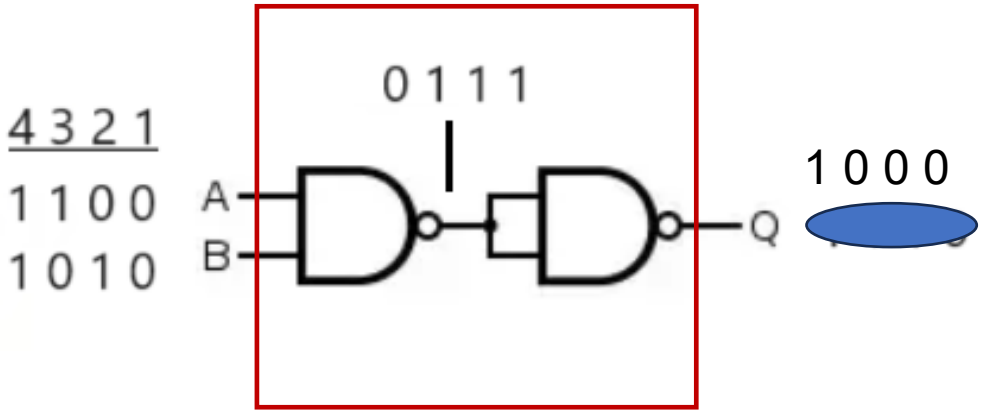
NOT

Truth table

A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

(b) : AND gate from NAND gates

AND



(c) : OR gate from NAND gates

OR

(d) : NOR gate from NAND gates

NOR

(e) : XOR gate from NAND gates

XOR

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