Digital Techniques

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Experiment No.2
Boolean algebra

1. Introduction

1.1 Objective:

To study the axioms defining Boolean algebra and how to represent Boolean expressions in POS (product- of – sums) form.

1.2 Theory:

Digital systems are composed of combinations of logic gates described by a truth table and Boolean expression or a logic symbol diagram. The fundamental Boolean identities for AND, OR and NOT operations can be summarized as follows: -

Table (2-1) Boolean expression

A+B=B+A	A. B=B.A
A+(B+C) =(A+B) +C	A. (B.C) = (A.B).C
A.(B+C) =A. B+A.C	A+B.C=(A+B). (A+C)
A+0=A	A.1=A
A+1=1	A.0=0
A+A=A	A. A=A
$A+\overline{A}.B=A+B$	A.(A+B) =A
A. B+A.C=A.(B+C)	(A+B). (A+C) =A+B.C

In combinational logic, the output of the circuit depends only on the inputs to the circuit. Combinational logic problems are normally given in the form of

logical statements or a truth table. To design and implement the problem, Boolean logical expressions (equations) are derived for the output logic function in terms of the binary variables representing the inputs. The logic expressions are given either in the forms of a sum of products (SOP) or in the form of a product of sums (POS).

Procedure:

1) Use Boolean algebra to simplify the following expressions. Then find the truth table for each after connecting the circuits.

a) $F_1 = A \cdot B + A \cdot (B + C) + B \cdot (B + C)$

b) $F_2 = \overline{A \cdot B} + A \cdot \overline{C} + B \cdot C$

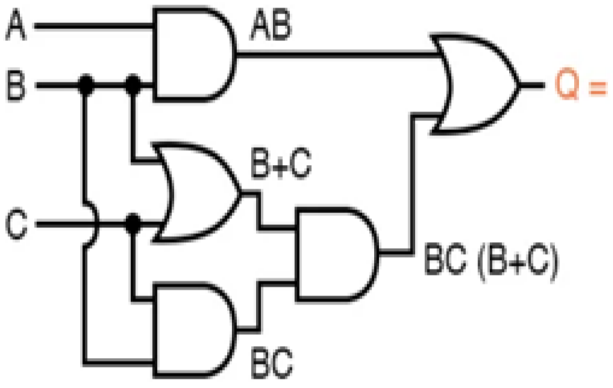
c) $F_3 = (A + \overline{B} + \overline{A \cdot B}) \cdot (\overline{A} + \overline{B})$

d) $F_4 = (A \oplus B) \oplus (B \oplus C)$

e) $F_5 = (A \otimes B) \otimes (B \otimes C)$

f) $F_6 = \overline{A} \cdot \overline{B} \cdot \overline{D} + A \cdot \overline{B} \cdot \overline{C} \cdot D + A \cdot \overline{B} \cdot C \cdot \overline{D}$

2. Use Boolean algebra to find Q ?



Discussion:

1. Determine whether or not the following equalities are correct:

(a) $A \cdot B \cdot C + \overline{A} \cdot B \cdot C = A$

(b) $A + B \cdot \overline{A} \cdot C = B \cdot C$

2. Find F for the circuit in Fig. (2-1)

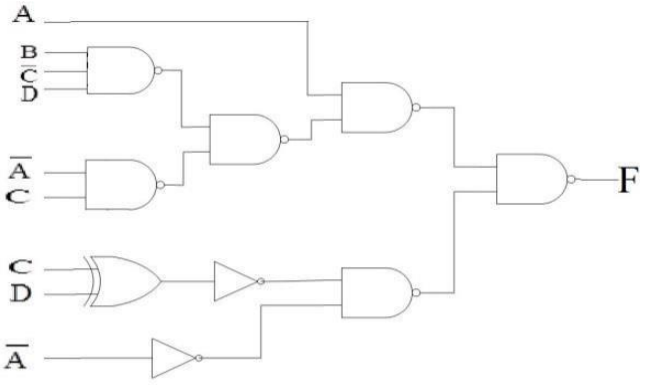


Fig. (2-1)