Microprocessor Architecture

Type of interrupts in 8085

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Type of interrupts in 8085

Interrupt is a process where an external device can get the attention of the microprocessor. The process starts from the I/O device.

*Interrupts can be classified into two types:

Maskable (can be delayed)

Non-Maskable (cannot be delayed)

*Interrupts can also be classified into

Vectored (the address of the service routine is hard-wired)

Non-vectored (the address of the service routine needs to be supplied externally)

Type of interrupts in 8085

- An interrupt is considered to be an emergency signal. The microprocessor should respond to it as soon as possible.

- When the Microprocessor receives an interrupt signal, it suspends the currently executing program and **jumps to an Interrupt Service Routine (ISR) to respond to the incoming interrupt. Each interrupt will most probably have its own ISR.**

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Responding to Interrupts

Responding to an interrupt may be immediate or delayed depending on whether the interrupt is maskable or non-maskable and whether interrupts are being masked or not.

There are two ways of redirecting the execution to the ISR depending on whether the interrupt is vectored or non-vectored. The vector is already known to the Microprocessor, while in the non-vectored type, the device will have to supply the vector to the Microprocessor

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The 8085 Interrupts

The maskable interrupt process in the 8085 is controlled by a single flip flop inside the microprocessor. This Interrupt Enable flip flop is controlled using the two instructions "EI" and "DI".

The 8085 has a single Non-Maskable interrupt. The non-maskable interrupt is not affected by the value of the Interrupt Enable flip flop.

The 8085 has 5 interrupt inputs:

1) The INTR input. The INTR input is the only non-vectored interrupt. INTR is maskable using the EI/DI instruction pair.

2) RST 5.5, RST 6.5, RST 7.5 are all automatically vectored. RST 5.5, RST 6.5, and RST 7.5 are all maskable.

3) TRAP is the only non-maskable interrupt in the 8085 TRAP is also automatically vectored.

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***An interrupt vector is a pointer to where the ISR is stored in memory.**

*All interrupts (vectored or otherwise) **are mapped onto a memory area called the Interrupt Vector Table (IVT).** The IVT is usually located in memory page 00(0000H -00FFH).
The purpose of **the IVT is to hold the vectors that redirect the microprocessor to the right place when an interrupt arrives. The IVT is divided into several blocks. Each block is used by one of the interrupts to hold its "vector"**

Interrupt name	Maskable	Vectored
INTR	Yes	No
RST 5.5	Yes	Yes
RST 6.5	Yes	Yes
RST 7.5	Yes	Yes
TRAP	No	Yes

Type of interrupts in 8085

The 8085 Non-Vectored Interrupt Procedure

1. The interrupt process should be enabled using the EI instruction.
2. The 8085 checks for an interrupt during the execution of every instruction.

3.If there is an interrupt, the microprocessor will complete the executing instruction, and start a RESTART sequence.

4. he RESTART sequence resets the interrupt flip flop and activates the interrupt acknowledge signal (INTA).

5. Upon receiving the INTA signal, the interrupting device is expected to return the op- code of one of the 8 RST instructions.

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6. When the microprocessor executes the RST instruction received from the device, it saves the address of the next instruction on the stack and jumps to the appropriate entry in the IVT.

7. The IVT entry must redirect the microprocessor to the actual service routine.

8. The service routine must include the instruction EI to re-enable the interrupt process.

9. At the end of the service routine, the RET instruction returns the execution to where the program was interrupted.