Lecture 10

Second Stage

Medical Physical Department

Digital Electronics

Lecture 10: Logic Families

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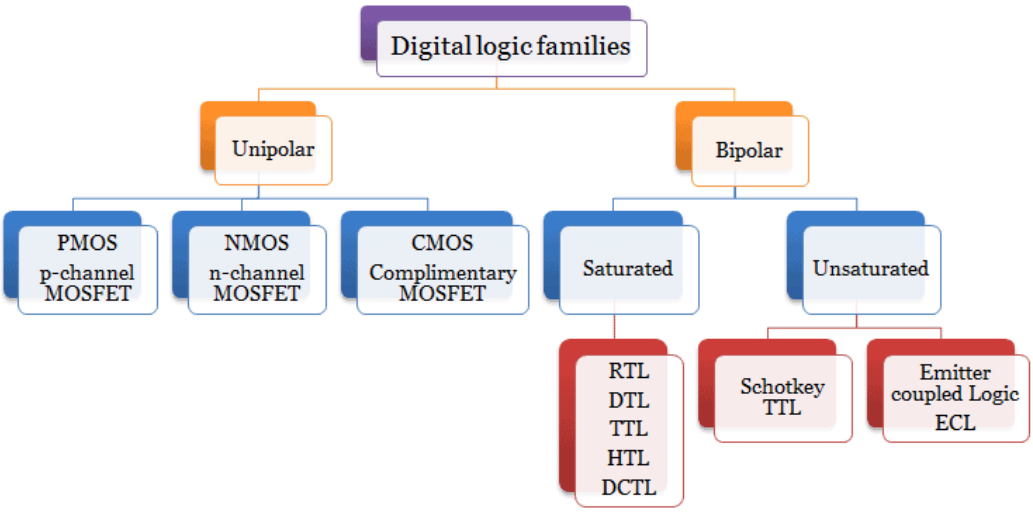
1. Logic Families

- It is a group of compatible ICs with the same logic levels and the supply voltages for performing various logic functions
- They are the building block of logic circuits.

2. Types of Logic Families



2.1 Bipolar ICs

1. The main element of a bipolar ICs are Resistors, Diodes, Capacitors and Transistors.
2. They can be operated in two ways:

1. **Saturated**
2. **Non-Saturated**

1. Saturated Logic: The transistors in the IC are driven to saturation

- Saturated Bipolar families are:
  - Resistor-Transistor logic (RTL),
  - Direct-Coupled transistor logic (DCTL),
  - Integrated-injection logic (IIL),
  - Diode-transistor logic (DTL),
  - High-Threshold logic (HTL) and
  - Transistor-transistor logic (TTL)

2. Non-Saturated Logic: The transistors in the IC are not driven to saturation.

- Non-Saturated Bipolar families are:

- Schottkey TTL
- Emitter-Coupled logic (ECL)

2.2 Unipolar Logic Families

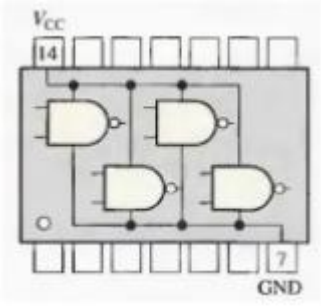
- ***Metal-Oxide-Silicon structure*** (MOS) devices are unipolar devices and only ***The metal–oxide–semiconductor field-effect transistor*** (MOSFETS) are employed in MOS logic circuits.
- These families are:
  - PMOS (p-channel MOSFETS)
  - NMOS (n-channel MOSFETS)
  - CMOS (Both p- and n- channel MOSFETS are fabricated on same silicon chip)

3. Basic Characteristics of ICs

- Propagation delay
- Power dissipation
- Fan in and fan out
- Noise immunity
- Power supply requirement
- Figure of merits i.e. speed power product
- Operating temperature
- Current and voltage parameters

Power Supply Requirement

- CMOS and TTL are available in different supply voltage categories
- In each IC, Vcc pin is connected to positive supply and GND pin is connected to ground of supply.



Current and voltage parameters

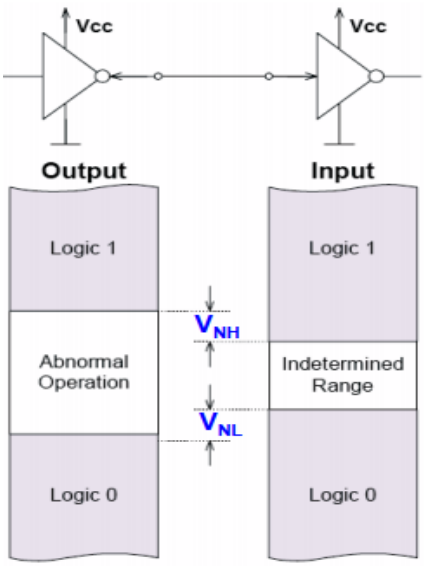
- Four different kind of Logic level specifications are defined: V_{IL}, V_{IH}, V_{oL}, V_{OH}

- V_{IL}, V_{IH}: These are the input logic levels (Low& High)
- V_{OL}, V_{OH}: These are the output logic levels (Low& High)

Noise Immunity

- Noise is unwanted voltage that is induced in electrical circuits and can cause threat to proper operation of circuit.
- Noise immunity is the ability to tolerate of unwanted voltage fluctuations on its inputs without changing certain amount outputs

Noise Margin



HI state noise margin:
$V_{NH} = V_{OH}(min) - V_{IH}(min)$

LO state noise margin:
$V_{NL} = V_{IL}(max) - V_{OL}(max)$

Noise margin:
$V_N = min(V_{NH}, V_{NL})$

In communications system engineering, noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

For example, a digital circuit might be designed to swing between 0.0 and 1.2 volts, with anything below 0.2 volts considered a '0', and anything above 1.0 volts considered a '1'. Then the *noise margin* for a '0' would be the amount that a signal is below 0.2 volts, and the *noise margin* for a '1' would be the amount by which a signal exceeds 1.0 volt. In this case noise margins are measured as an absolute voltage, not a ratio. Noise margins for CMOS chips are usually much

greater than those for TTL because the $V_{OH\ min}$ is closer to the power supply voltage and $V_{OL\ max}$ is closer to zero.

- Real digital inverters do not instantaneously switch from a logic high (1) to a logic low (0), there is some capacitance. While an inverter is transitioning from a logic high to low, there is an undefined region where the voltage cannot be considered high or low. This is considered a noise margin. There are two noise margins to consider:
  Noise margin high (N_{MH}) and noise margin low (N_{ML}). N_{MH} is the amount of voltage between an inverter transitioning from a logic high (1) to a logic low (0) and vice versa for N_{ML}. The equations are as follows: $N_{MH} \equiv V_{OH} - V_{IH}$ and $N_{ML} \equiv V_{IL} - V_{OL}$. Typically, in a CMOS inverter V_{OH} *will equal* V_{DD} (supply voltage) and V_{OL} will equal the ground potential, as mentioned above.

Power Dissipation تبديد الطاقة

This is the amount of power dissipated in an IC.

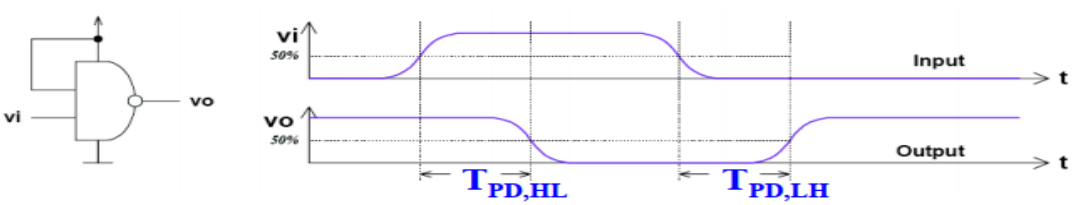
It is determined by the Supply Current Icc, that it draws from the Supply Volatge Vcc supply, and is given by,

$$\mathbf{Pd=V_{cc} \times I_{cc}.}$$

Propagation Delay

Electrical engineers need to take propagation delay into account when creating integrated circuits (ICs). In this context, propagation delay is defined as the amount of time required after an input signal is applied and has stabilized to the input of a circuit to the time that the output of the circuit has stabilized to the correct output signal. This is symbolized as t_{pd}. It can also be called *gate delay* and is more related to the amount of time it takes for the individual components,

called *logic gates*, to change than the time for the signal to move from one point to another.



$T_{PD,HL}$ – input-to-output propagation delay from HI to LO output
$T_{PD,LH}$ – input-to-output propagation delay from LO to HI output

Speed-power product: $T_{PD} \times P_{avg}$

Fan in and Fan out

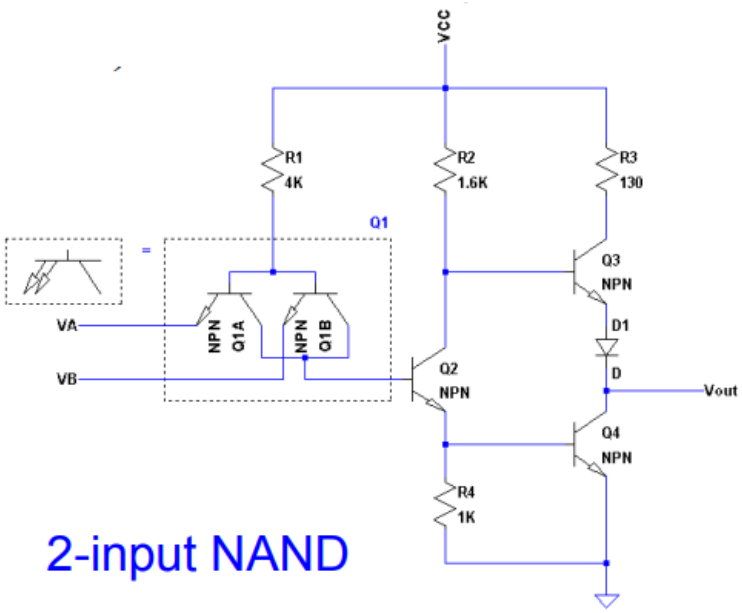
- Fan in and Fan out Fan-in: Number of inputs a gate has. For example, a two input gate will have fan-in equal to 2
- Fan-out: Maximum number of inputs of the same IC family that a gate can drive without falling outside the specified output voltage limits.

4. Transistor-Transistor Logic (TTL)

- first introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Standard TTL family (e.g. 7400) is obsolete
- Newer TTL families still used (e.g. 74ALS00)

Distinct features

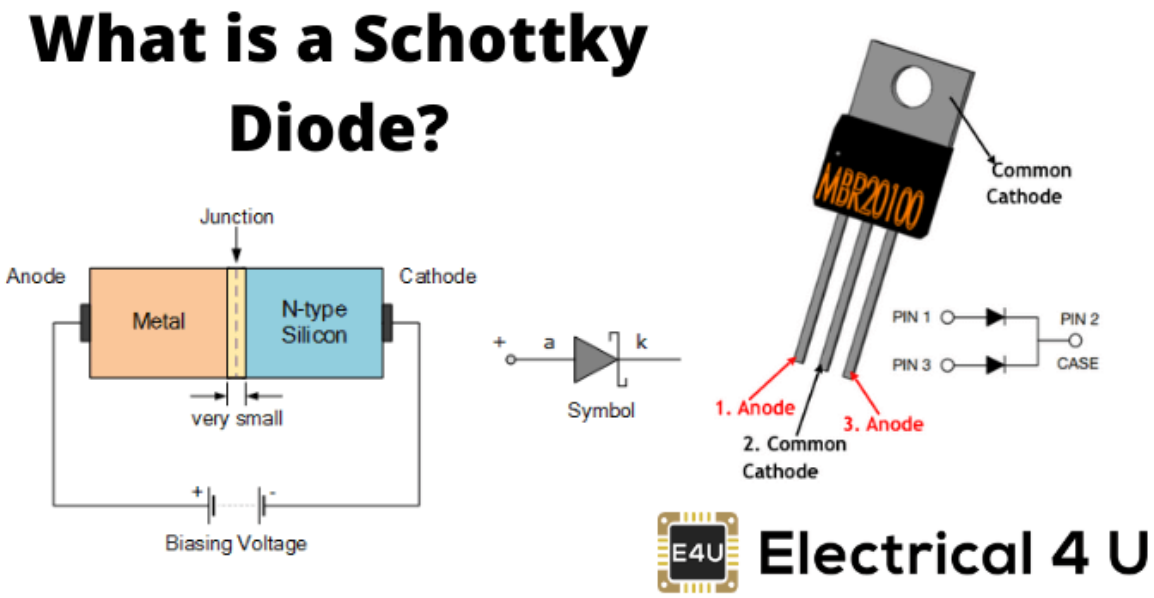
- Multi-emitter transistors
- Totem-pole transistor arrangement
- Open LTspice example: T
- .TL NAND…



4.1 TTL evolution

Schottky series (74LS00) TTL

The Low Power Schottky (LS TTL) logic IC family is similar in function to the original 7400 series TTL family. It has the same propagation delay as the 7400 series, but current and power reduction are improved by a factor of 5. This is accomplished by using Schottky diode clamping to prevent saturation and advanced processing. 74LS IC's were used very widely in the 70's, 80's, and 90's, and devices in this family were available in a wide range of functions. The devices can operate between 7.75 and 5.25 VDC,m with 2mw typical dissipation. Typical gate delay is 10 ns. *Most of these devices are now discontinued.*



A major slowdown factor in Bipolar junction transistor (BJTs) is due to transistors going in/out of saturation

• Shottky diode has a lower forward bias (0.25V)

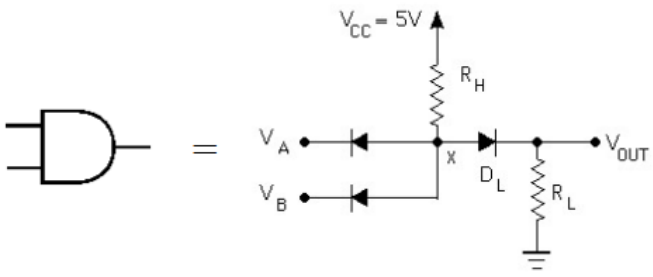
• When BC junction would become forward biased, the Schottky diode bypasses the current preventing the transistor from going into saturation

5. Diode Logic (DL)

Diode logic (DL), or diode-resistor logic (DRL), is the construction of Boolean logic gates from diodes.

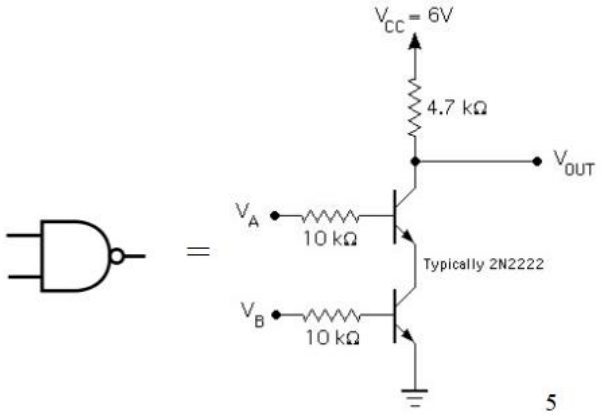
•simplest; does not scale

•NOT not possible (need an active element)



6. Resistor-Transistor Logic (RTL)

• replace diode switch with a transistor switch
• can be cascaded
• large power draw



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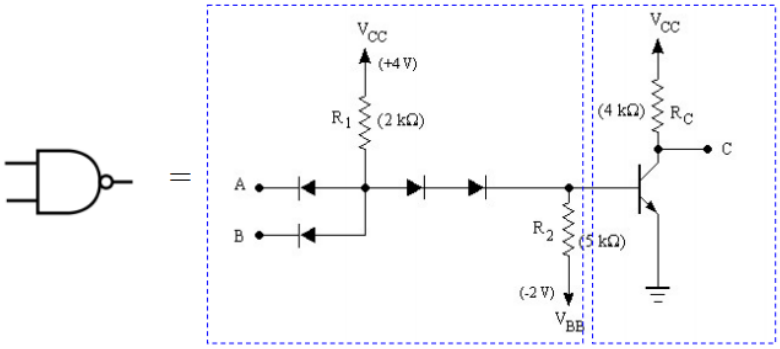
7. Diode-Transistor Logic (DTL)

• essentially diode logic with transistor amplification
• reduced power consumption
• faster than RTL



DL AND gate Saturating inverter

8. Complimentary MOS (CMOS)

- Other variants: NMOS, PMOS (obsolete)
- Very low static power consumption
- Scaling capabilities (large integration all MOS)
- Full swing: rail-to-rail output
- Things to watch out for:
  – don't leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
  – susceptible to electrostatic damage (finger of death)
- Open LTspice example: CMOS NOT and NAND
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3. Comparison of IC Digital Logic Families

Table 1: Comparison of Main IC Digital Logic Families

S.N.	Parameter	DTL	HTL	TTL	RTL	ECL	MOS	CMOS
1.	Basic Gates (Positive Logic)	NAND	NAND	NAND	NOR	OR-NOR	NAND	NOR or NAND
2.	Fan out (Minimum)	8	10	10	5	24	20	>50
3.	Typical power dissipation per gate, mW	8-12	55	12-22	12	40-55	0.2-10	0.01 static 1 at 3 MHz
4.	Noise immunity	Good	Excellent	Very good	Medium	Good	Medium	Very good
5.	Typical propagation delay/gate, ns	30	90	12-6	12	4-1	300	70
6.	Clock rate (minimum frequency at which flip-flops operate), MHZ	12-30	4	15-60	8	60-400	2	5
7.	Number of functions	Fairy High	Medium	Very high	high	High	Low	Low