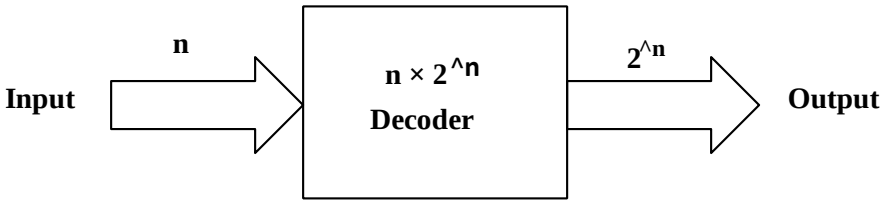
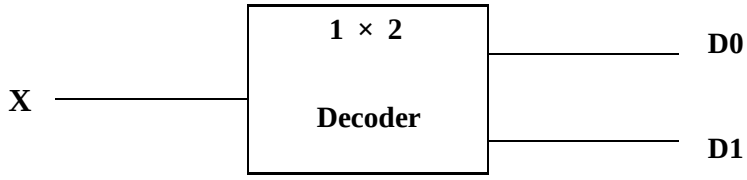
1. ***Decoders:*** is a Combinational Logic Circuit that convert Binary information from (n) input line to a maximum of 2^n unique output line.

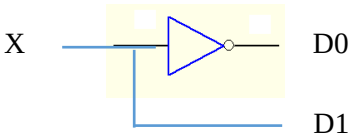


EX1: **Design One to two Decoder**



1-2 Decoder

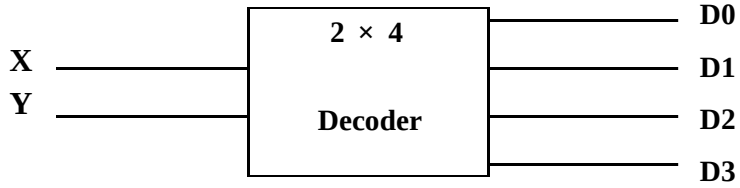
X	D0	D1
0	1	0
1	0	1



$D0 = \overline{X}$

D1 = X

EX2: **Design Two to Four Decoder**



X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

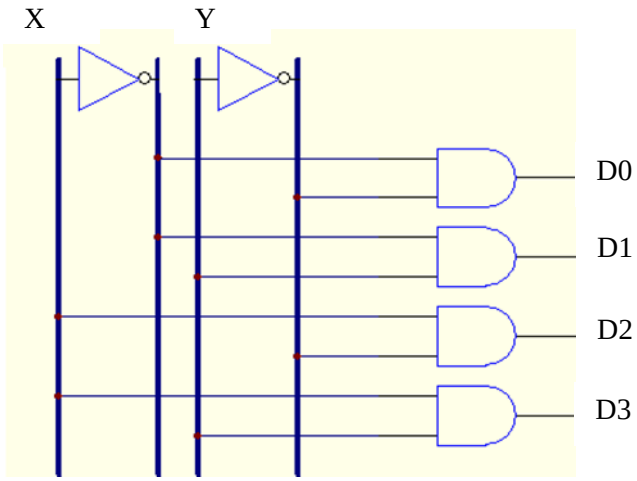
Two to Four Decoder Truth Table

$D0 = \overline{X}\,\overline{Y}$

$D1 = \overline{X}\,Y$

$D2 = X\,\overline{Y}$

$D3 = X\,Y$



Ex3: **Design 3-8 Decoder**

C	**B**	**A**	**y0**	**y1**	**y2**	**y3**	**y4**	**y5**	**y6**	**y7**
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

$y0 = \overline{C}\,\overline{B}\,\overline{A}$

$y1 = \overline{C}\,\overline{B}\,A$

$y2 = \overline{C}\,B\,\overline{A}$

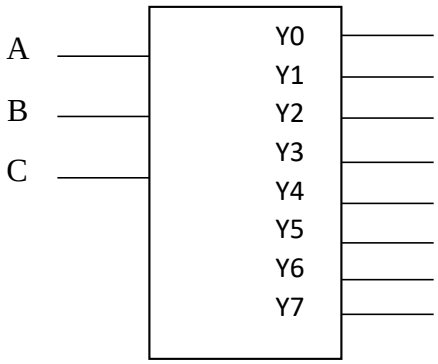
$y3 = \overline{C}\,B\,A$

$y4 = C\,\overline{B}\,\overline{A}$

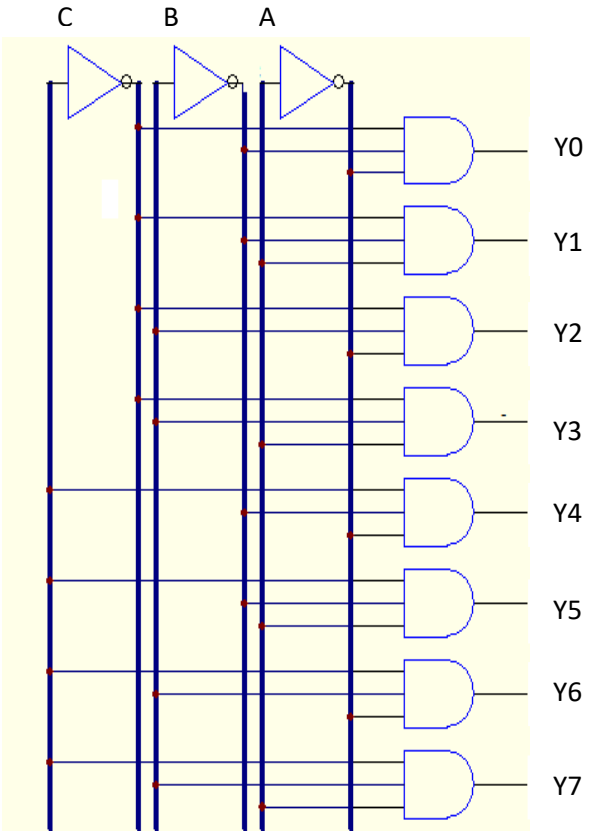
$y5 = C\,\overline{B}\,A$

$y6 = C\,B\,\overline{A}$

$y7 = C\,B\,A$



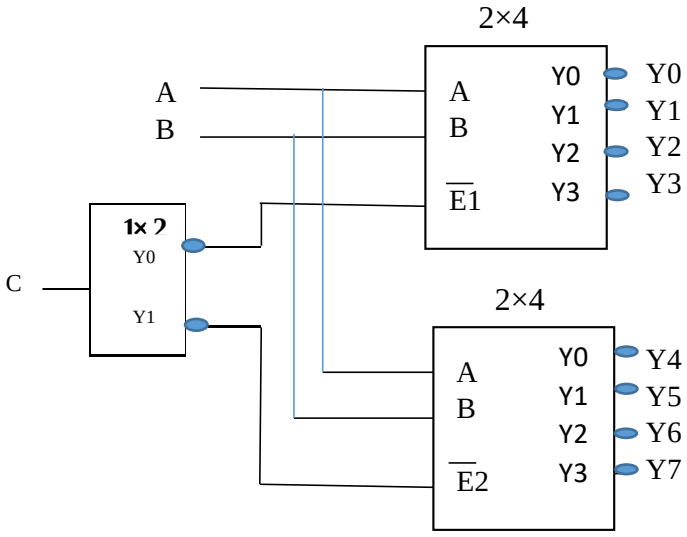
3-8 Decoder



* Note: all the previous decoders are active high outputs but the most popular decoders are active low outputs.

Ex4: Design 3-8 decoder using 2 of(2-4 decoders)and one (1-2 decoder), with active low output.

Important note: We use Enable input to expanded decoders.



C	E2	E1	B	A	Y4	Y5	Y6	Y7	Y0	Y1	Y2	Y3
0	0	1	0	0	0	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1
0	0	1	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	0	1	1	1	1
1	1	0	0	0	1	1	1	1	0	1	1	1
1	1	0	0	1	1	1	1	1	1	0	1	1
1	1	0	1	0	1	1	1	1	1	1	0	1
1	1	0	1	1	1	1	1	1	1	1	1	0