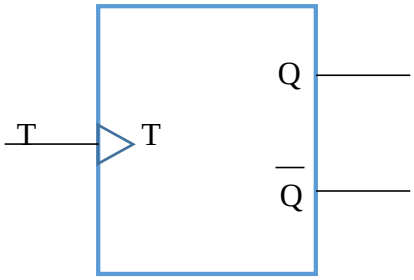
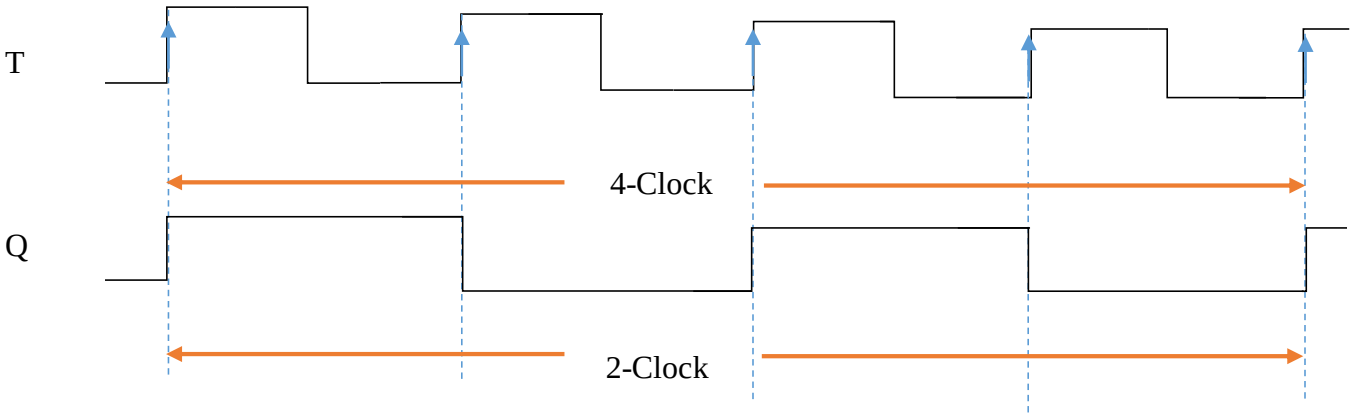
Counter

A counter is a device which can count any particular event on the basis of how many times the particular event(s) is occurred.

Asynchronous Counters:

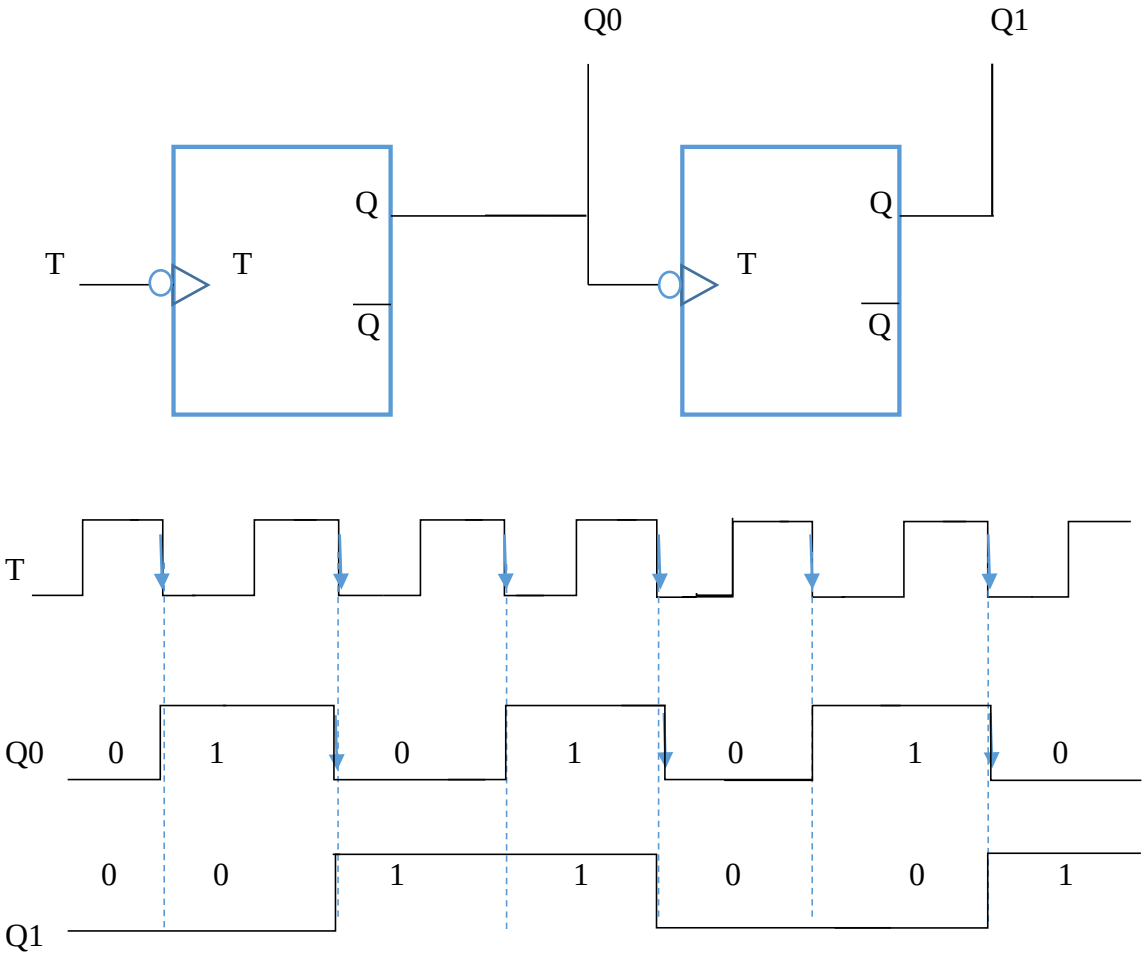
The term asynchronous refers to events that do not have a fixed time relationship with each other and, generally, do not occur at the same time. An asynchronous counter is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.



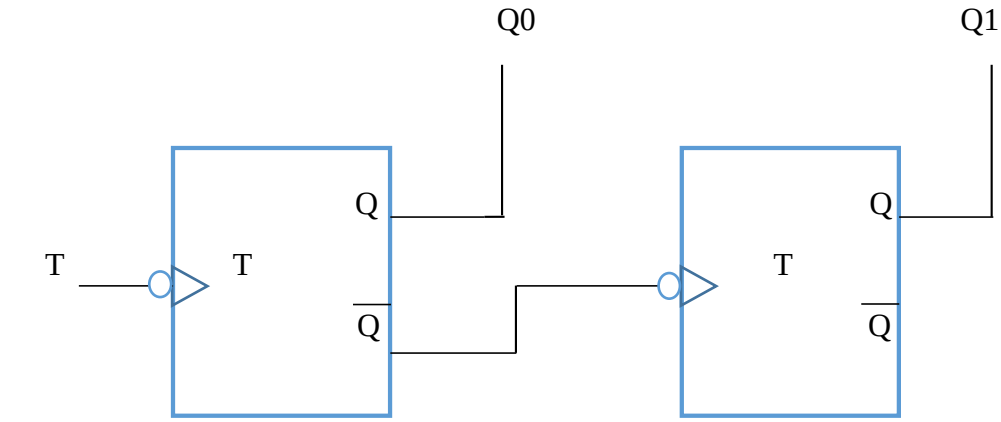


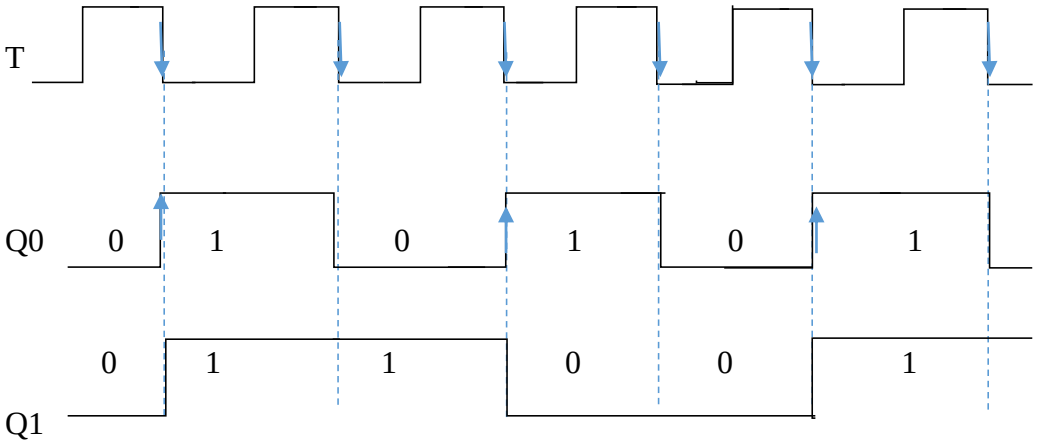
*T-Flip Flop is use to divide the input frequency of digital signal by 2.

2-Bit Binary Asynchronous Up Counter:

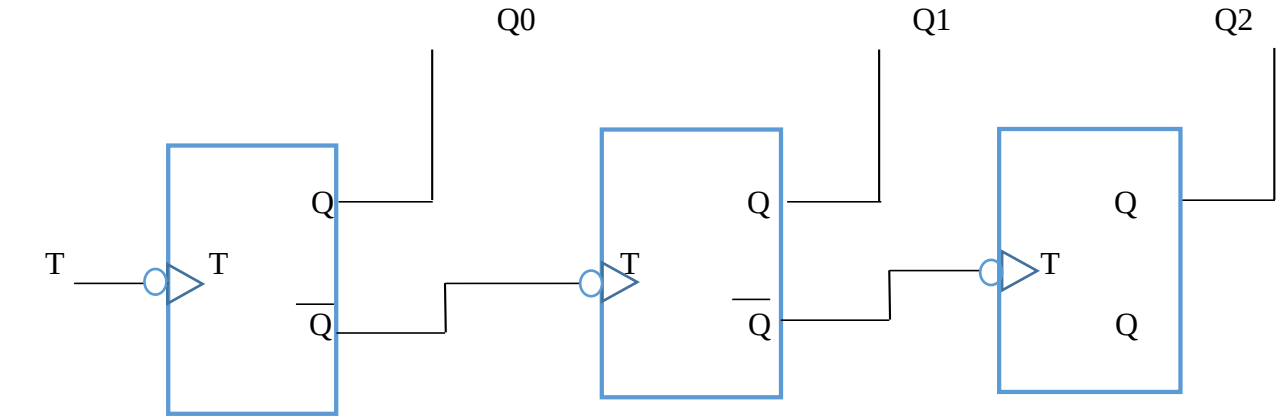


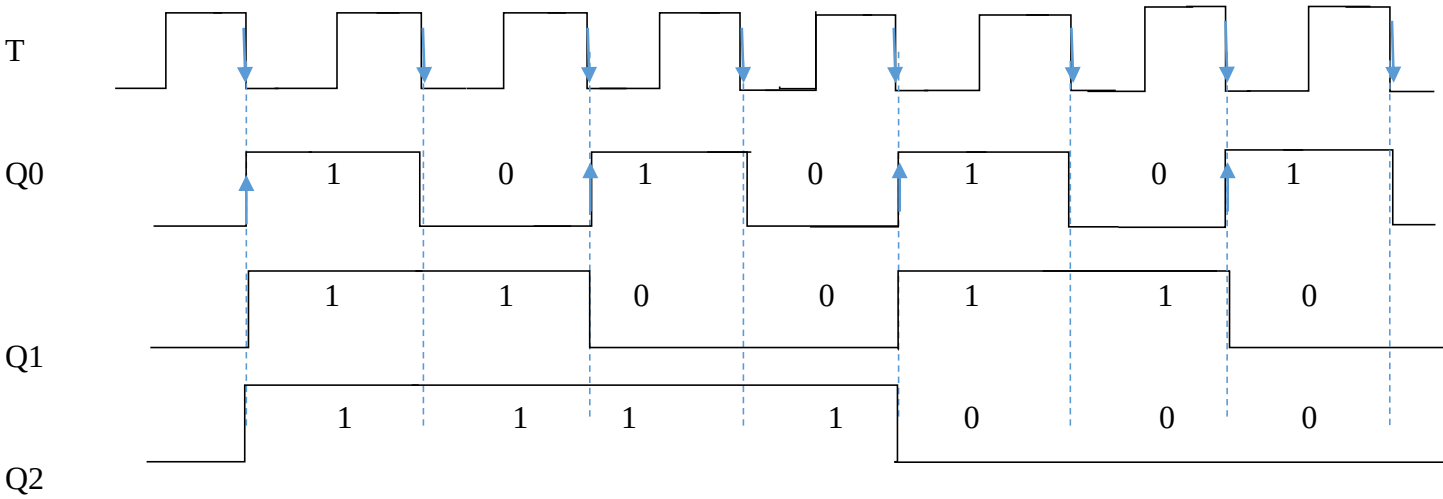
2-Bit Binary Asynchronous Down Counter:



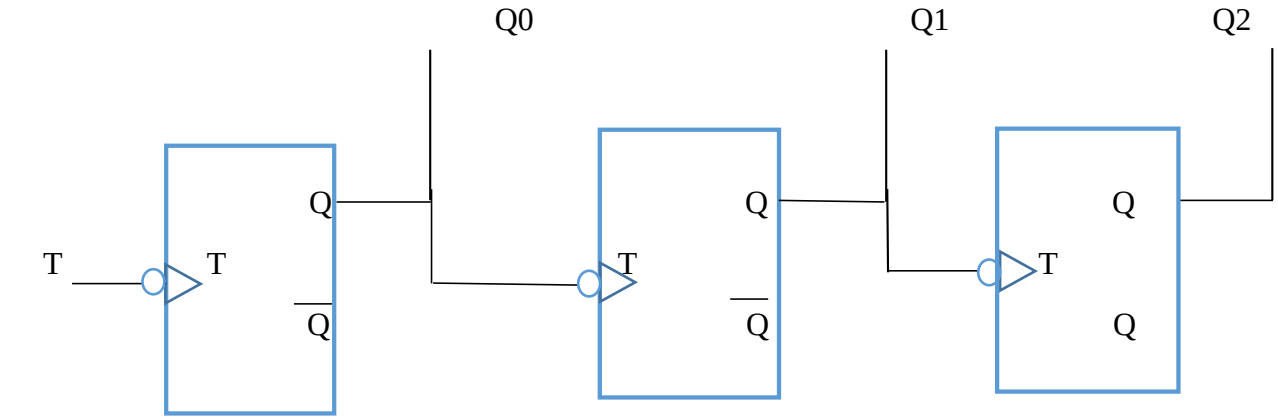


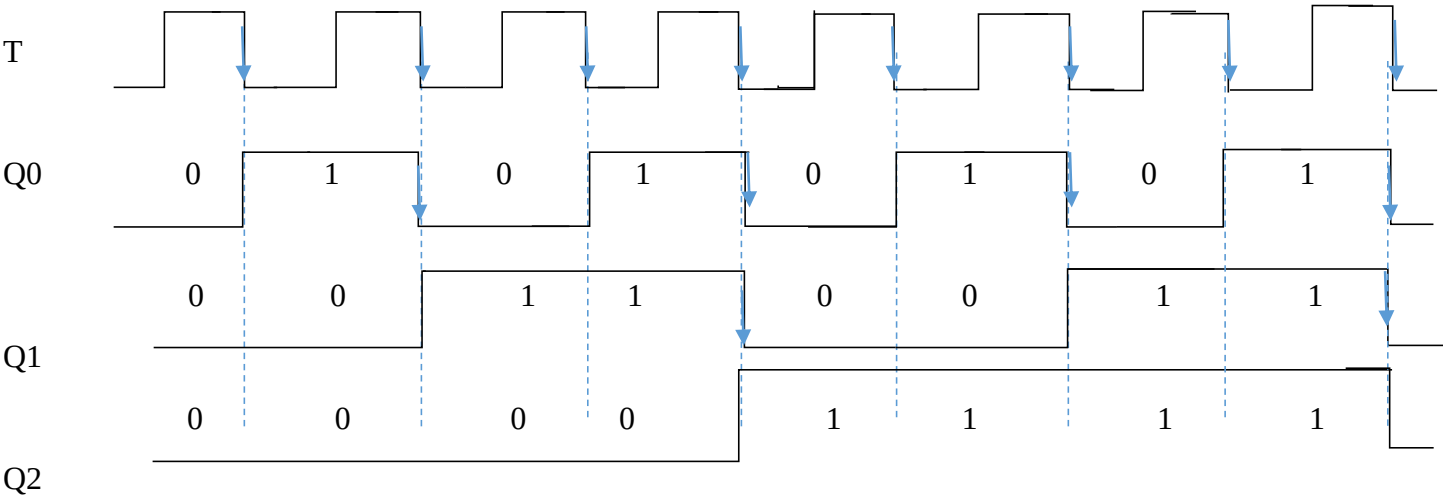
Ex1: Design 3-bit binary asynchronous down counter and draw timing diagram.





Ex2: Design 3-bit binary asynchronous up counter and draw timing diagram.

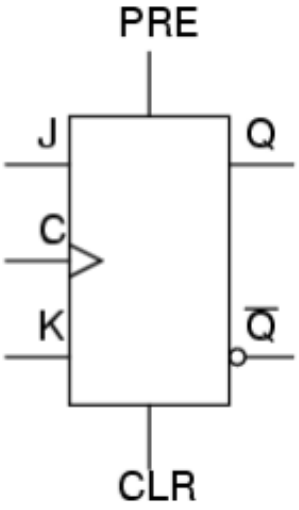


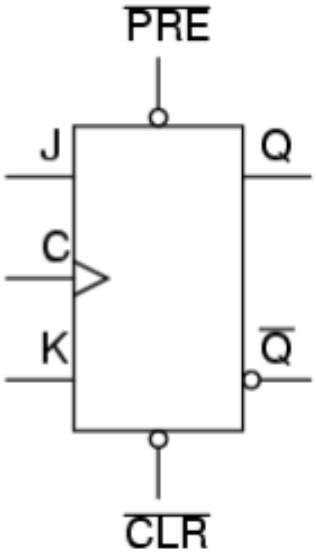


Counter Modification: When the **preset** input is activated, the flip-flop will be set (Q=1, not-Q=0) regardless of any of the synchronous inputs or the clock. When the clear input is activated, the flip-flop will be reset (Q=0, not-Q=1), regardless of any of the synchronous inputs or the clock.

Preset and clear inputs find use when multiple flip-flops are ganged together to perform a function on a multi-bit binary word, and a single line is needed to set or reset them all at once. Asynchronous inputs can be engineered to be active-high or active-low. If they're active-low, there will be an inverting bubble at that input lead on the block symbol, just like the negative edge-trigger clock inputs.

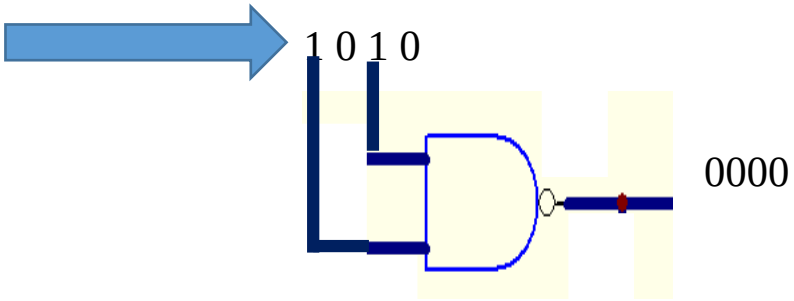
Sometimes the designations "PRE" and "CLR" will be shown with inversion bars above them, to further denote the negative logic of these inputs:

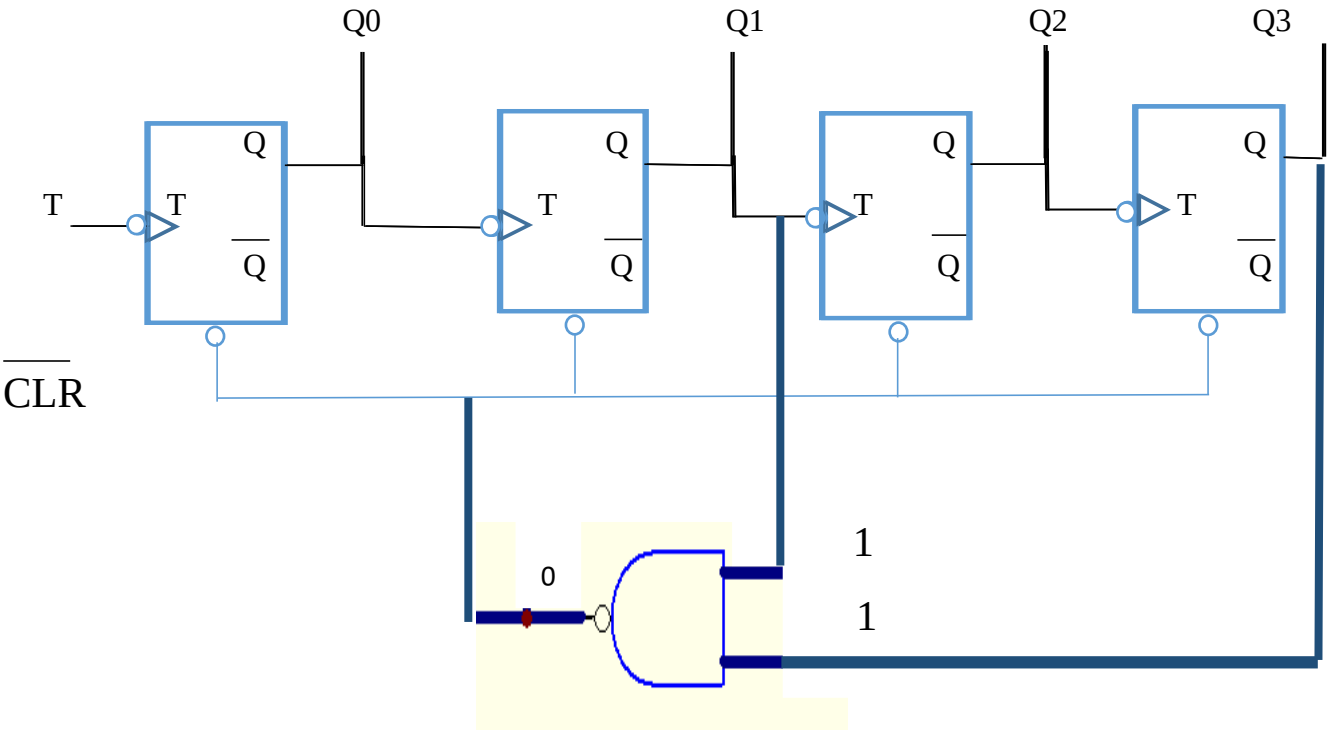




Ex3: Design “Asynchronous” BCD up counter, count from (0 to 9)

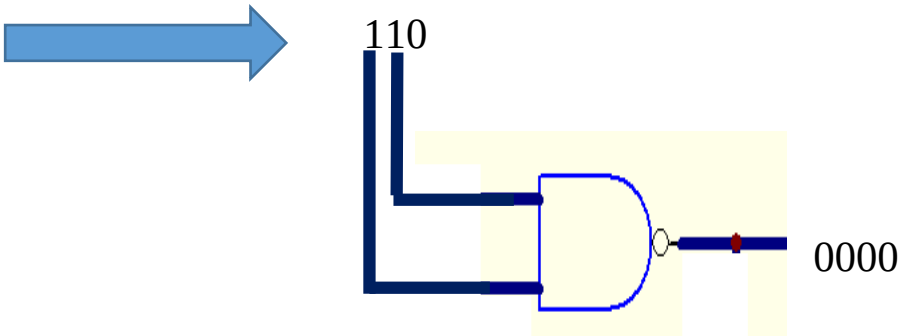
Q3	Q2	Q1	Q0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

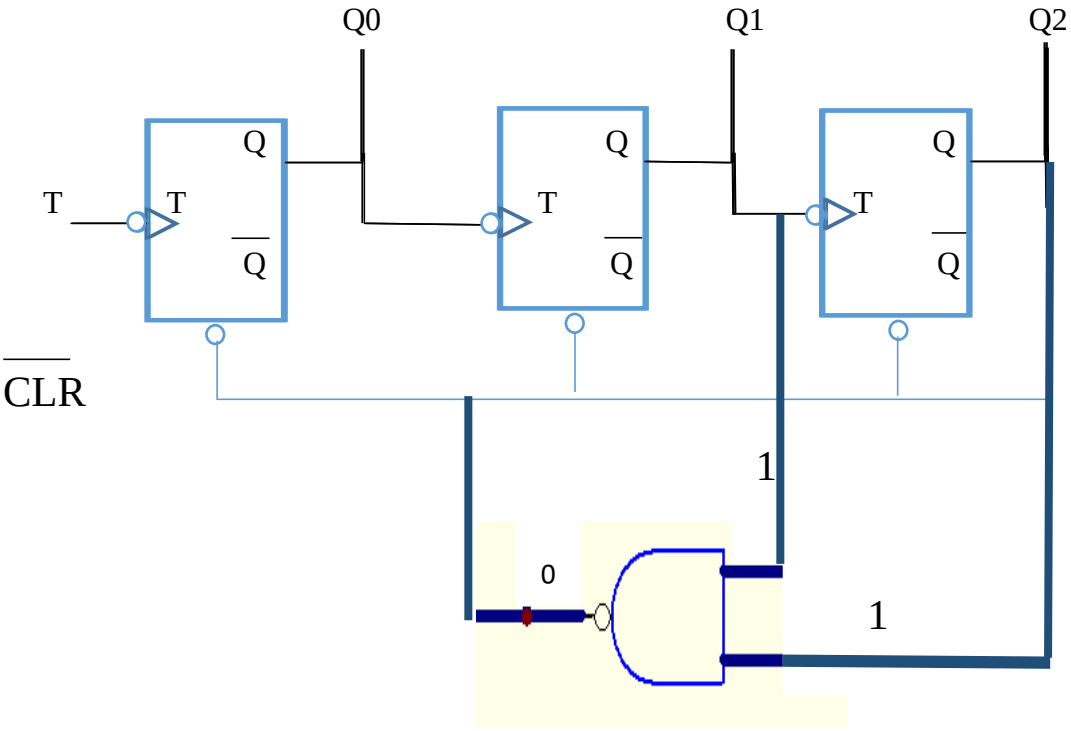


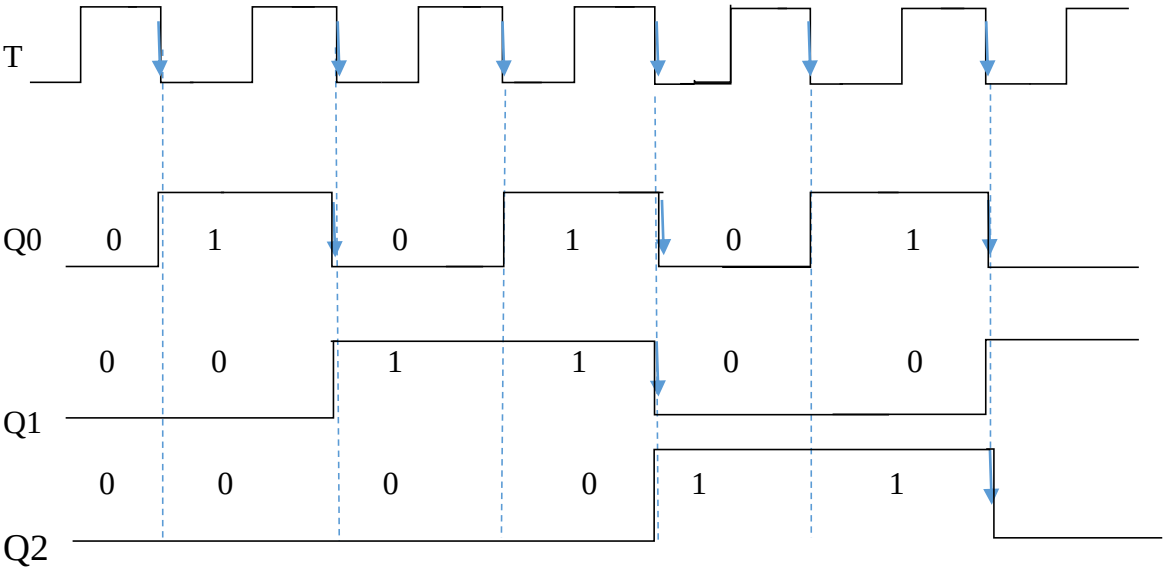


Ex4: Design “Asynchronous” up counter, to count from (0 to 5) and draw timing digram.

Q2	Q1	Q0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

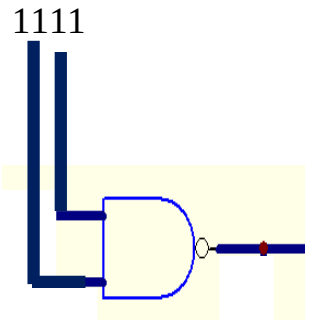


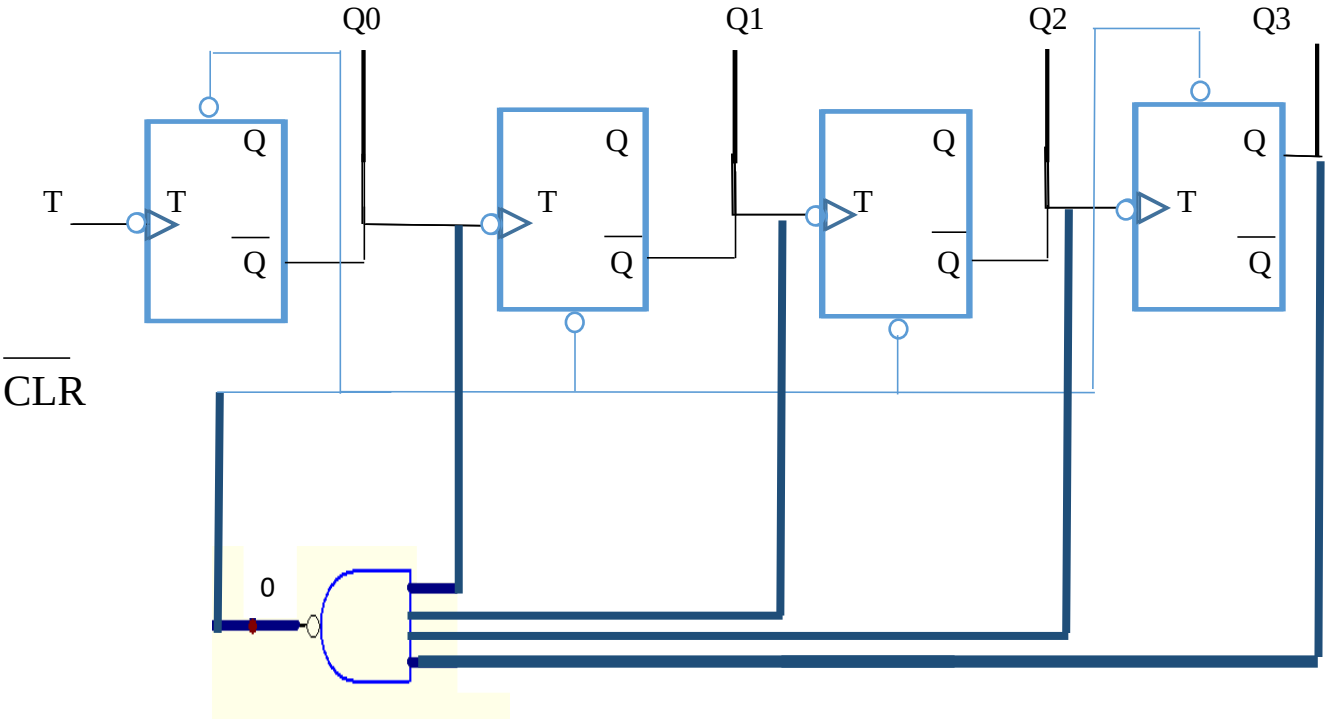

Q0
Q1
Q2
T
T
Q
Q
T
T
Q
Q
T
T
Q
Q
CLR
1
0
1


T
Q0
0
1
0
1
0
1
Q1
0
0
1
1
0
0
Q2
0
0
0
0
1
1

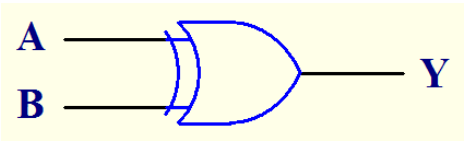
Ex5: Design “Asynchronous” BCD down counter, count from (9 to 0)

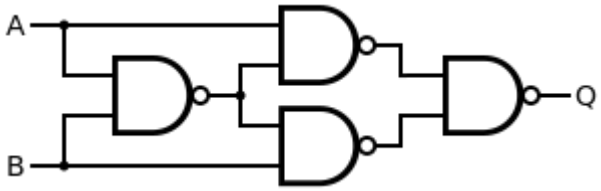
Q3	Q2	Q1	Q0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0





6. XOR (Exclusive OR)gate:



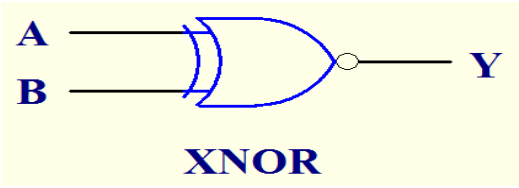


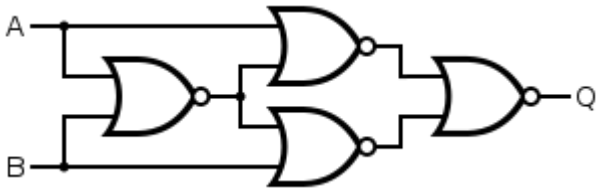
Truth table:

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Boolean expression:
Y=A'B+AB'=A⊕B

7. XNOR(Exclusive NOR)gate:





Truth table:

INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Boolean expression:
Y=A'B'+AB= (A⊕B)'