## **Multiplexer**

(MUX for short) is a Combinational circuit that selects binary information from one of many input lines and directs it to single output line.

## Multiplexer parts:

- 1- Selection lines
- 2- Input lines
- 3- Output line



Note: MUX is decoder ("Active high outputs") with AND & OR gates

## Ex1: Design 4-to-1-line Multiplexer



Ex2: Design 8-to-1-line Multiplexer



| S | 2 S 1 | I SC | ) Y |
|---|-------|------|-----|
| 0 | 0     | 0    | IO  |
| 0 | 0     | 1    | I1  |
| 0 | 1     | 0    | I2  |
| 0 | 1     | 1    | I3  |
| 1 | 0     | 0    | I4  |
| 1 | 0     | 1    | I5  |
| 1 | 1     | 0    | I6  |
| 1 | 1     | 1    | I7  |







H.W: Design 8-1 MUX using  $2 \times (4-1 \text{ MUX})$  and  $1 \times (2-1 \text{ MUX})$ 



Ex4: Design 16-1 MUX using  $2 \times (8-1 \text{ MUX})$  and  $1 \times (2-1 \text{ MUX})$ 

## Demultiplexer

The demultiplexer (DEMUX) is a combinational logic circuit designed to switch one common input line to one of several separate output line

Demultiplexer Output Line Selection:





| Ŧ | Select    |            | O/P            |    |                |    |  |
|---|-----------|------------|----------------|----|----------------|----|--|
|   | <b>S1</b> | <b>S</b> 0 | D <sub>0</sub> | D1 | D <sub>2</sub> | D3 |  |
| 1 | 0         | 0          | 1              | 0  | 0              | 0  |  |
| 1 | 0         | 1          | 0              | 1  | 0              | 0  |  |
| 1 | 1         | 0          | 0              | 0  | 1              | 0  |  |
| 1 | 1         | 1          | 0              | 0  | 0              | 1  |  |

