# Latches and Flip-Flops

Logic circuits are classified into two main types:

- **Combinational** Circuit is the type of circuit in which output is independent of time and only relies on the input present at that particular instant.
- **Sequential** circuit is the type of circuit where output not only relies on the current input but also depends on the previous output.

- **R'-S' Latch:**

R'-S' Latch
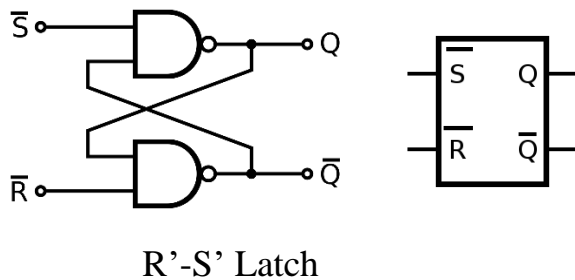
$\overline{S}$	$\overline{R}$	Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	1*	1*	Undefined
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q_n	$\overline{Q_n}$	No change

R-S Latch
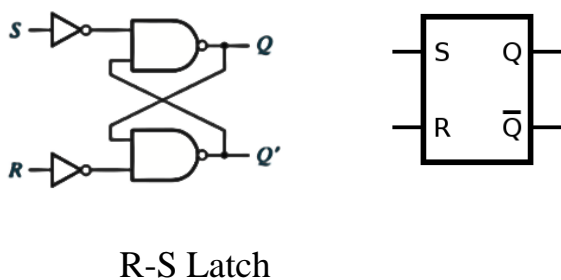
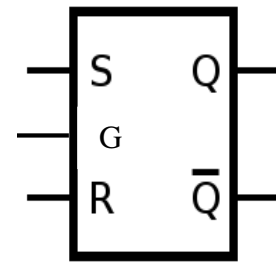| S	R	Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	Q_n	$\overline{Q_n}$	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	1*	1*	Undefined

- **Gated S-R Latch**

  A gated latch requires an enable input, EN (G is also used to designate an enable input). The logic diagram and logic symbol for a gated S-R latch are shown below. The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input. The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs. The gated latch is a

level-sensitive device. In this circuit, the invalid state occurs when both S and R are simultaneously HIGH and EN is also HIGH.
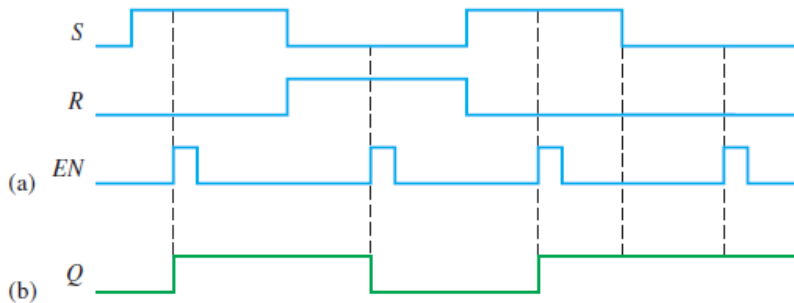

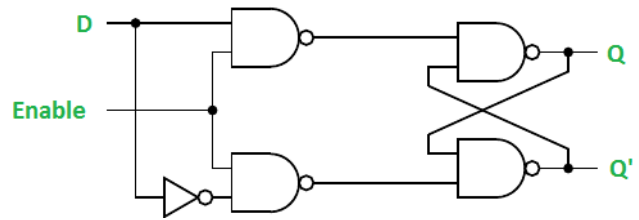| G	S	R	Qn+1	$\overline{Qn+1}$	
0	X	X	Qn	$\overline{Qn}$	No change
1	0	0	Qn	$\overline{Qn}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1*	1*	Undefined

Gated R-S Latch

Determine the Q output waveform if the inputs shown in Figure (a) are applied to a gated S-R latch that is initially RESET.
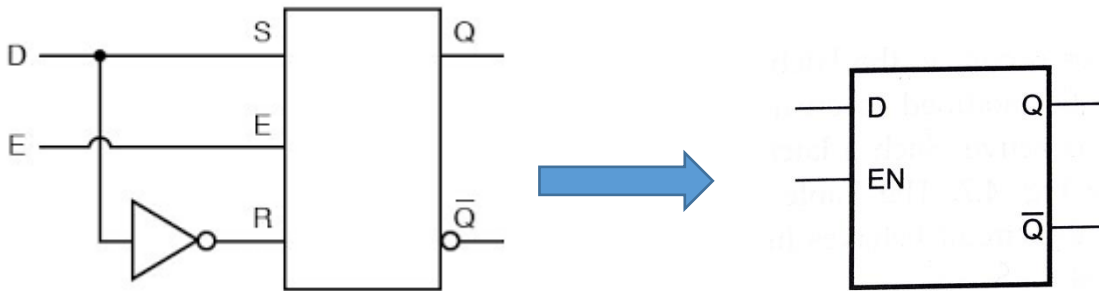

(a)

Solution (b)

• D-Latch

| E	D	Qn+1	$\overline{Qn+1}$
0	X	Qn	$\overline{Qn}$
1	0	0	1
1	1	1	0

D-Latch

• Master-Slave Flip-Flops

A master-slave flip-flop is normally constructed from two flip-flops: one is the Master flip-flop and the other is the Slave. In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted CP is given to the slave flip-flop. For example, if the CP=0 for a master flip-flop, then the output of the inverter is 1, and this value is assigned to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop.

When CP=1, the master flip-flop is enabled and the slave flip-flop remains isolated from the circuit until CP goes back to 0. Now Y and Y' depends on the external inputs R and S of the master flip-flop.
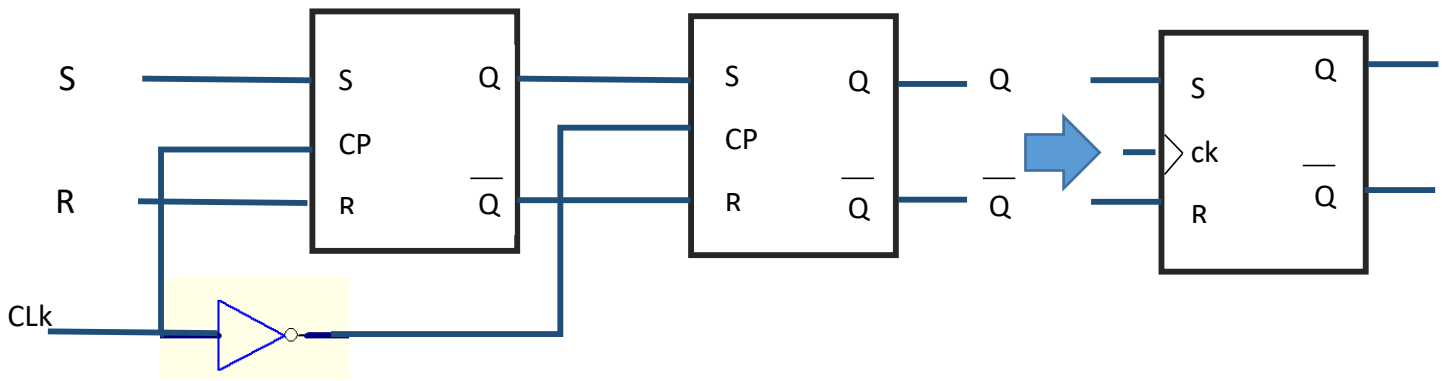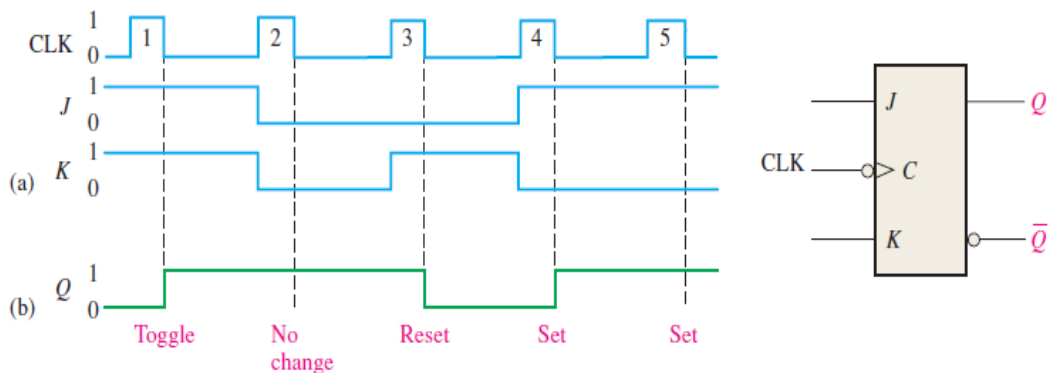
R-S Flip- Flip

- ## The J-K Flip-Flop

The J and K inputs of the J-K flip-flop are synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. When J is HIGH and K is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET. When J is LOW and K is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET. When both J and K are LOW, the output does not change from its prior state. When J and K are both HIGH, the flip-flop changes state. This called the toggle mode. This basic operation of a positive edge-triggered flip-flop is illustrated in Figure below, and Table below is the truth table for this type of flip-flop. Remember, the flip-flop cannot change state except on the triggering edge of a clock pulse. The J and K inputs can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output.
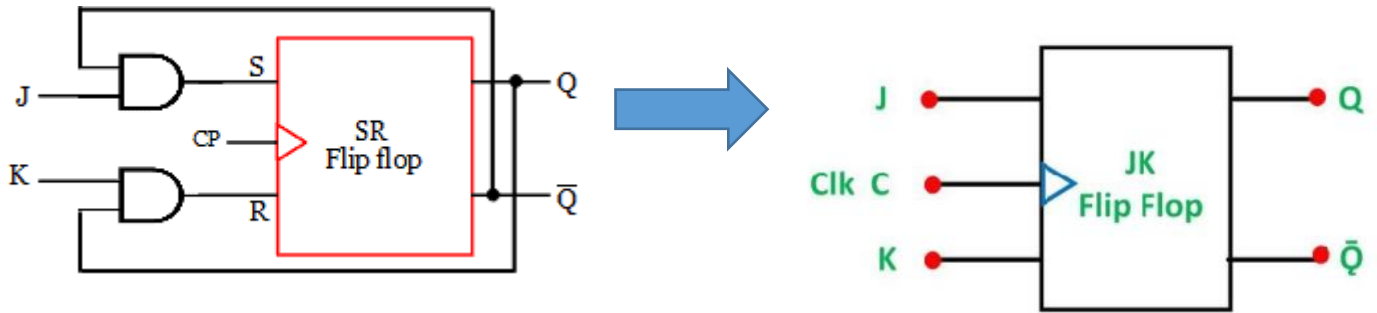
CP	J	K	Qn+1	$\overline{Qn+1}$	
0	X	X	Qn	$\overline{Qn}$	No change
1	0	0	Qn	$\overline{Qn}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\overline{Qn}$	Qn	Toggle

The waveforms in Figure are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.
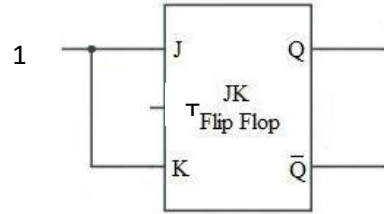

- ## **The Toggle (T) Flip Flop**

The name T flip-flop is termed from the nature of toggling operation. The major applications of T flip-flop are counters and control circuits. T flip flop is modified form of RS flip-flop making it to operate in toggling region.

Whenever the clock signal is LOW, the input is never going to affect the output state. The clock has to be high for the inputs to get active.

T	Qn+1	$\overline{Qn+1}$	
----	Qn	$\overline{Qn}$	No change
↑	$\overline{Qn}$	Qn	Toggle

T- Flip Flop