Al-Mustaqbal University College
Department of Medical Instrumentation Techniques Engineering
Class: Three
Subject: Medical electronic system
Lecturer: Dr. zahraa hashim kareem
Second semester/ Lecture-3: DAC performance calculation

Performance Characteristics of Digital to Analog Converter

Settling time

Settling Time: time required for the output to fall with in $\pm\frac{1}{2}V_{LSB}$ when a change occurs in the input code.

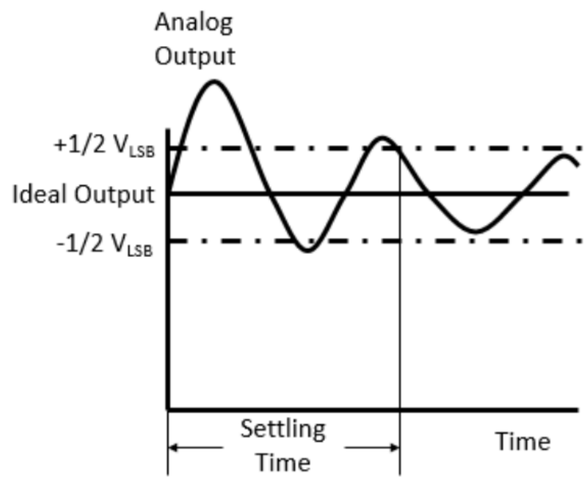

Figure 3.33

DAC Performance Calculations

- To calculate <u>LSB full-scale output</u>:

$$\boldsymbol{Full\ scale\ (LSB) = \frac{1}{2^n} \times 100\%}$$

- To find the step size if you given the full-scale output

$$\boldsymbol{step\ size = \frac{Full - scale\ output}{2^n - 1}}$$

- If you not given the full-scale output, then:

$$\boldsymbol{step\ size = resolution}$$

- To fine the analogue output (voltage or current output for a given digital input:

$$\boldsymbol{Analogue\ output = (Digital\ input)_{10} \times step\ size}$$

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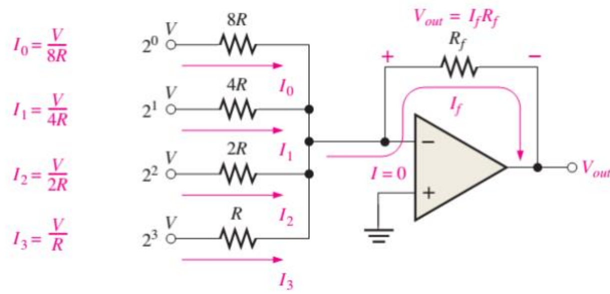
Example 10 Assume 4-bits Binary-Weighted-Input DAC in Figure below.

a. With $V_{ref} = 5\ V$, $R = 20\ k\Omega$, $R_F = 10\ k\Omega$, determine the step size and the full-scale voltage at V_{OUT}.

b. Change the value of R_F so that the full-scale voltage at V_{OUT} is $-2\ V$.

Solution



a.

$$resolution = \frac{1}{2^n} = \frac{1}{2^4} = 0.0625$$

$$step\ size = 0.0625 \times 5\ V = 0.3125\ V$$

$$full - scale\ output = -R_f\left[\frac{D_3}{R} + \frac{D_2}{2R} + \frac{D_1}{4R} + \frac{D_0}{8R}\right]$$

$$= -10\ k\Omega\left[\frac{5\ V}{20\ k\Omega} + \frac{5\ V}{40\ k\Omega} + \frac{5\ V}{80\ k\Omega} + \frac{5\ V}{160\ k\Omega}\right]$$

$$= \mathbf{-4.6875\ V}$$

b.

$$\frac{-2\ V}{-4.6875\ V} = \frac{R_f}{10\ k\Omega}$$

$$R_f = \mathbf{4.27\ k\Omega}$$

Example 11 A 10-bit DAC has a clock frequency of $1\ MHz$, a full-scale output of $10.23\ V$. Find:

a. The digital equivalent (in binary) required to produce $3.728\ V$.

b. The conversion time.

c. The resolution of this converter.

Solution

a.

$$step\ size = \frac{full - scale\ output}{2^n - 1}$$

$$step\ size = \frac{10.23\ V}{2^{10} - 1} = \mathbf{10\ mV}$$

$$number\ of\ steps = \frac{output\ voltage}{step\ size}$$

$$number\ of\ steps = \frac{3.7281\ V}{10\ mV} \cong \mathbf{373\ steps}$$

The digital equivalent required to produce 3.728 V is $(373)_{10}$

$$(373)_{10} = \mathbf{(0101110101)_2}$$

b.

373 steps required to complete the conversion.
The frequency of conversion is 1 MHz means the clock time (every step time) will take 1 μs.
So, the conversion time = $\mathbf{373\ \mu s}$.

c.

The resolution of this converter is:

$$\frac{1}{2^{10} - 1} \times 100\% = \mathbf{0.1\ \%}$$

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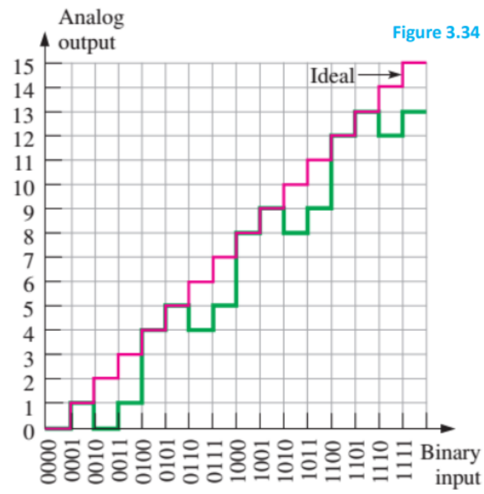
Digital-to-Analog Conversion Error

Nonmonotonicity

- The step reversals indicate ***nonmonotonic*** performance, which is a form of nonlinearity.
- In this particular case, the error occurs because the 2^1 bit in the binary code is interpreted as a constant 0.
- That is, a short is causing the bit input line to be stuck **LOW**.

Figure 3.34



Differential Nonlinearity

- Figure 3.35 illustrates ***differential nonlinearity*** in which the step amplitude is less than it should be for certain input codes.
- This particular output could be caused by the 2^2 bit having an insufficient weight, perhaps because of a faulty input resistor.
- We could also see steps with amplitudes greater than normal if a particular binary weight were greater than it should be.

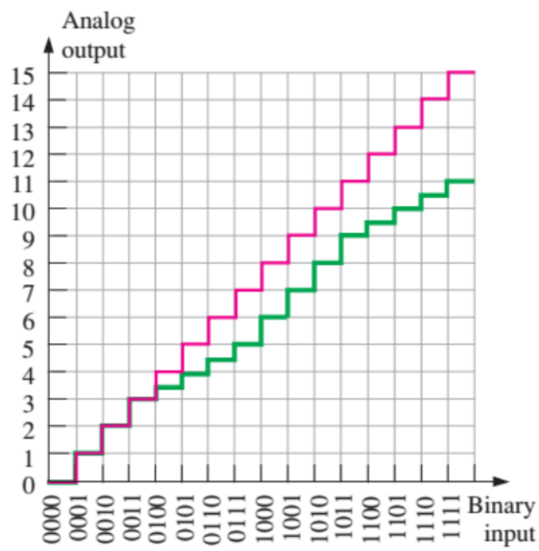


Figure 3.35

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Offset Error

- Notice that when the binary input is 0000, the output voltage is nonzero and that this amount of offset is the same for all steps in the conversion.
- A faulty op-amp may be the culprit in this situation.

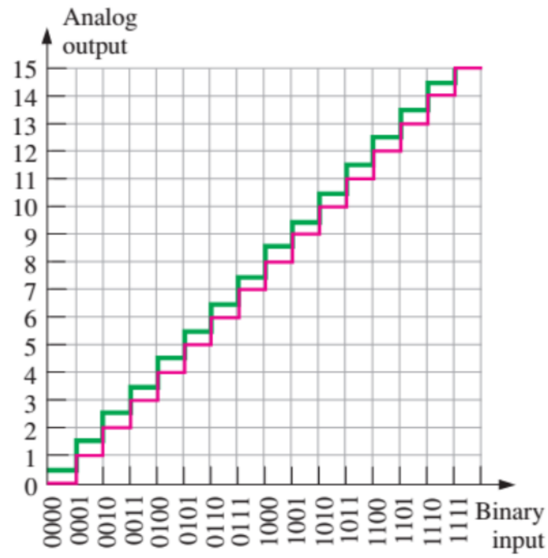

Figure 3.37

Low or High Gain

- In the case of low gain, all of the step amplitudes are less than ideal.
- In the case of high gain, all of the step amplitudes are greater than ideal.
- This situation may be caused by a faulty feedback resistor in the op-amp circuit.

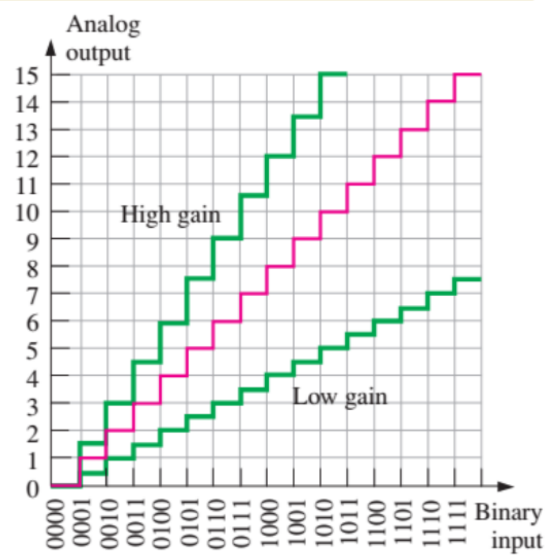

Figure 3.36

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