Al-Mustaqbal University College
Department of Medical Instrumentation Techniques Engineering
Class: Second
Subject: Measurements & Medical Transducers
Lecturer: Suhair Hussein, F.Diyaaldeen, Shahlaa yaseen
Experiment :3

Clamping Circuits

The instrument comprises of the following built in parts:

1- One DC regulated power supply of 0-3V.

2- Different types of resistance and capacitors are provided on the front panel according to the requirement of the circuits as shown in the engraved diagrams on the lab panels.

Theory

Clamping circuits:

A clamping circuit should not change the peak-to-peak value of the signal, it should only change the D.C. level. To do so, a clamping circuit uses a capacitor, together with a diode and a resistor**.**

1- Positive clamper: -

In a positive clamper fig (1), during the negative half cycle of the signal,
the diode is forward biased and shorts out the resistor RL. The time constant (= RC) will be about zero because the resistance of the forward biased diode is zero. Consequently, the capacitor charges to - Vm volts almost instantaneously and stays at that level for the entire negative half cycle. During the positive half cycle of the signal, the signal is +Vm volts. The diode is reverse biased so that capacitor tries to discharge through the resistor RL. In other words,

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the signal has been pushed upward by +Vm volts so that negative peaks fall on the zero level.

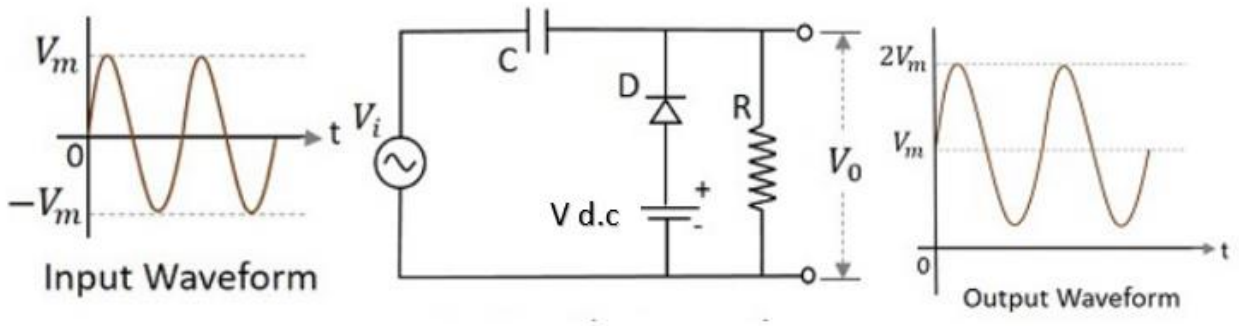

Fig (1). positive clamper

2- Negative clamper:

In a negative clamper fig (2), during the positive half cycle of the signal,
the diode is forward biased and shorts out the resistor RL. The time constant (= RC) will be about zero because the resistance of the forward biased diode is zero. Consequently, the capacitor charges to + Vm volts almost instantaneously and stays at that level for the entire positive half cycle. Whereas during the negative half cycle of the signal, the signal is -Vm volts. The diode is reverse biased so that capacitor tries to discharge through the resistor RL. Output still has peak-to-peak value of about 2Vm but is centred around -Vm volts instead of zero. In other words, the signal has been pushed downward by Vm volts so that positive peak lies on the zero level.

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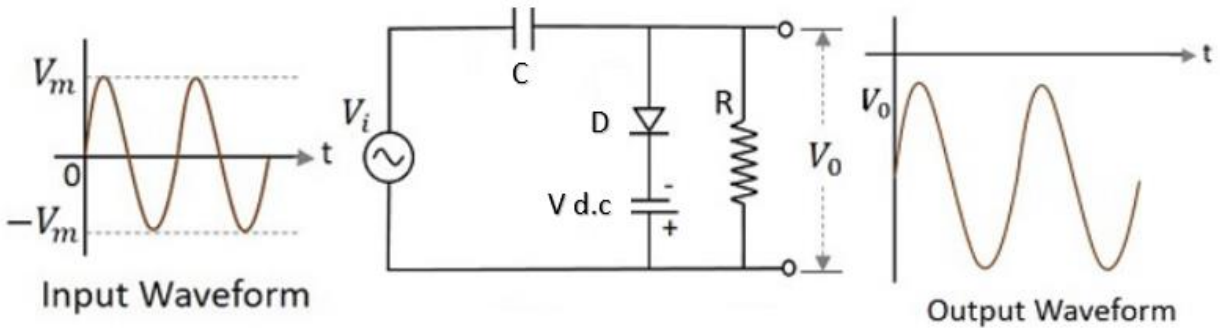

Fig(2). Negative clamper

Procedure

FOR POSITIVE CLAMPING CIRCUIT:

1- Apply input signal of 2V P-P. 1KHz from function generator at input terminals. Also connect CRO at output.

2- Set CRO at DC level.

3- Connect 3V DC regulated power supply.

4- Switch ON the instrument using ON/ OFF toggle switch provided on the front panel.

5- Check the output waveshape at CRO. When we increase the voltage we will observe that the DC level of the sine wave is shifted upward i.e. in positive side.

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FOR NEGATIVE CLAMPING CIRCUIT:

1- Apply input signal of 2V P-P. 1KHz from function generator at input terminals. Also connect CRO at output.

2- Set CRO at DC level.

3- Connect 3V DC regulated power supply.

4- Switch ON the instrument using ON/ OFF toggle switch provided on the front panel.

5-Check the output waveshape at CRO. When we increase the voltage we will observe that the DC level of the sine wave is shifted downward i.e. in negative side

Discussion:

1- **What is the relationship between the clamping level and the DC voltage?**
2- **If the variable DC source is reversed, how does this affect the clamping?**
3- **What is the use of the capacitor and its function in the clamper circuit?**