عنوان المحا ضرة:Input/output(RD,WR)

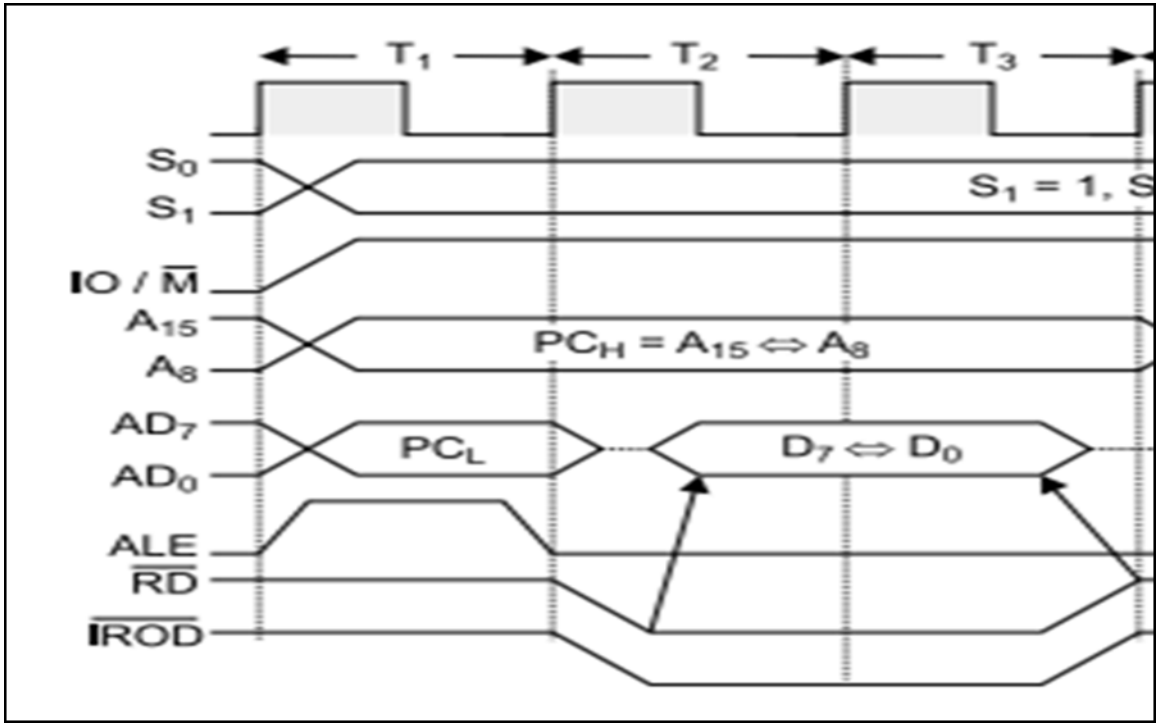
مادة :المعمارية

المرحلة :الثانية

استاذ المادة: Msc.Shuhub Ahmed

I/O Read:

Figure (5): I/O Read timing diagram



Operation:

1- It is used to fetch one byte from an IO port.

Operation

2- It requires 3 T-States.

3- During T1, The Lower Byte of IO address is duplicated into higher order address bus A8-A15.

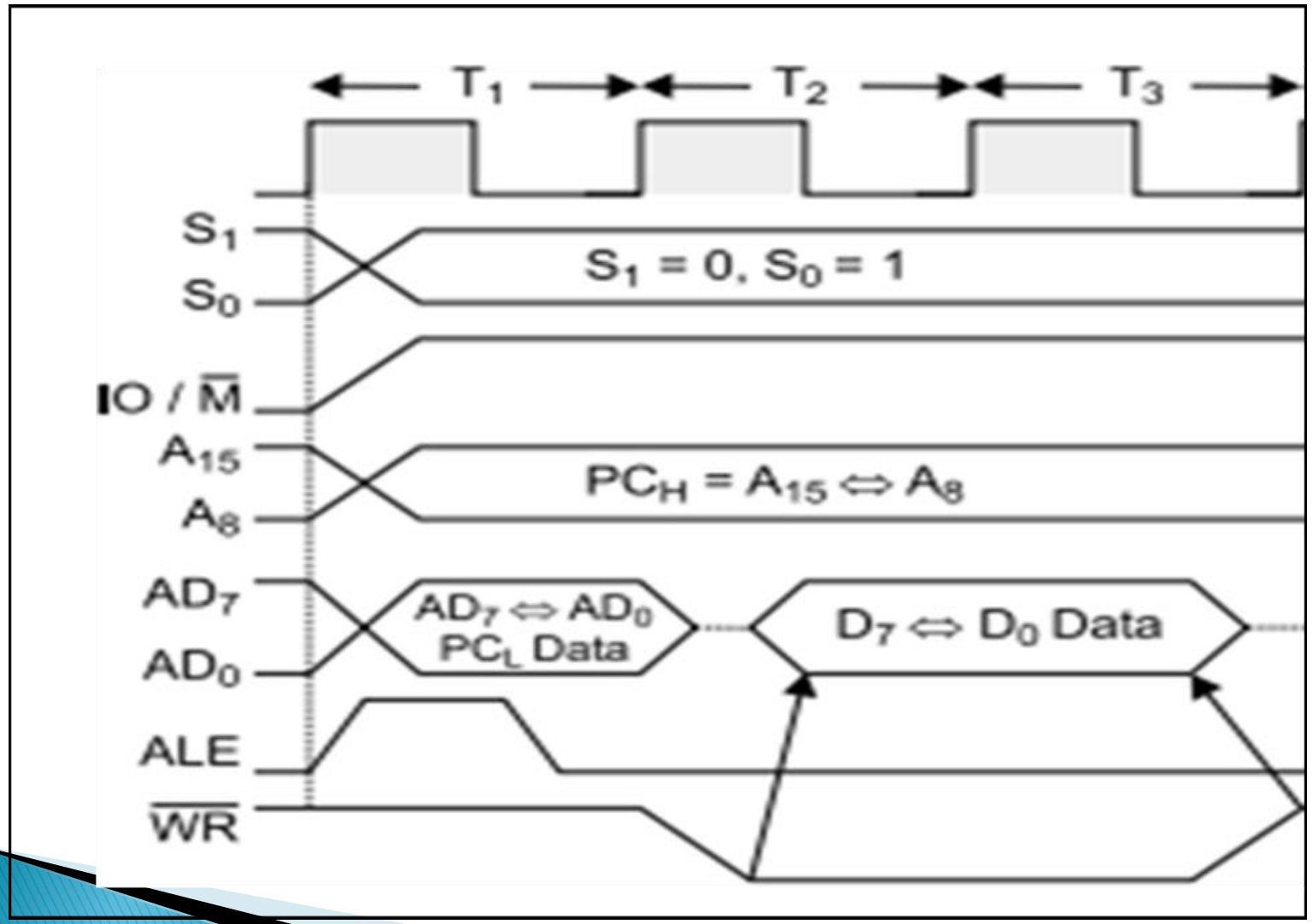
4- ALE is high and AD0-AD7 contains address of IO device.

5- IO/M $\overline{}$ goes high as it is an IO operation.

6-During T2 & T3, ALE goes low, $\overline{RD}$ goes low and data appears on AD0-AD7 as input from IO device.

IO Writ:

Figure (6): I/O Write timing diagrame:



Operation:

1- It is used to writ one byte to the IO device.

2- It requires 3 T-States.

3- During T1, the lower byte of address is duplicated into higher order address bus A8-A15.

4- ALE is high and A0-A7 address is selected from AD0-AD7.

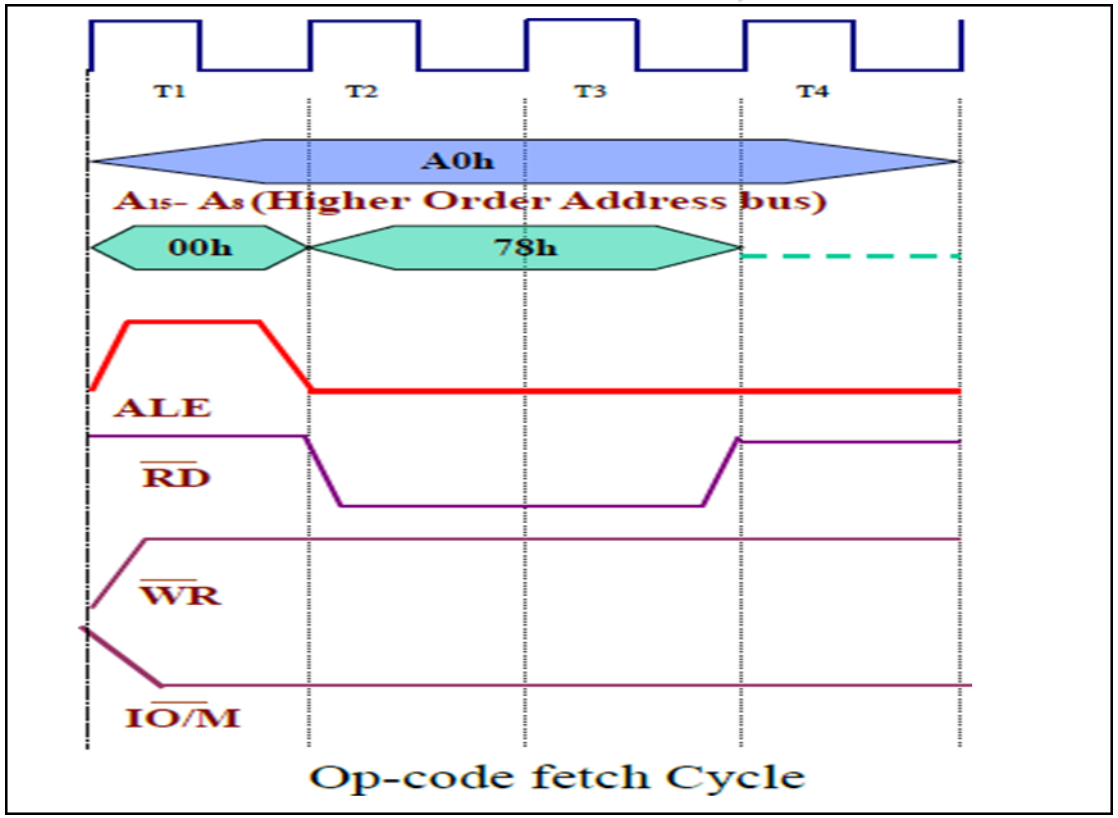
5-As it is an IO operation IO/M $\overline{}$ goes high.

6-During T2 & T3, ALE goes low, $\overline{WR}$ goes low and data appears on AD0-AD7 to write data to the IO device.

Examples:

1.A000 MOV A,B 78

(1 Byte instruction, 1 machine cycle == opcode fetch == 4T state)



Op-code fetch Cycle

OPERATION:

This 1 byte instruction and needs 1 machine cycle (opcode fetch). During T1, the content of the program counter (PC) is placed on the A8-A15 and AD0-AD7 as ALE goes high. During T2 & T3 of op code fetch cycle (M1), the op code of the instruction is loaded in the instruction register (IR). The T4-state of this cycle M1 is for decoding and the contents of B is copied in A.