LECTURE 9

Active Clamping Circuits

Analog Electronics

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By

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Outline and Aim

After completing this lecture, you should be able to:

- Describe the operation of an active clamping circuit
- Describe the operation of an active positive clamper with nonzero reference

An Active Clamping Circuit

A positive clamper with an op-amp and a diode is shown in Fig. 5.

This circuit overcomes a couple of disadvantages of the passive clamper.

- The use of the op-amp eliminates the peak found in the positive passive clamper output.
- It prevents loading the input source when the diode is forward-biased.

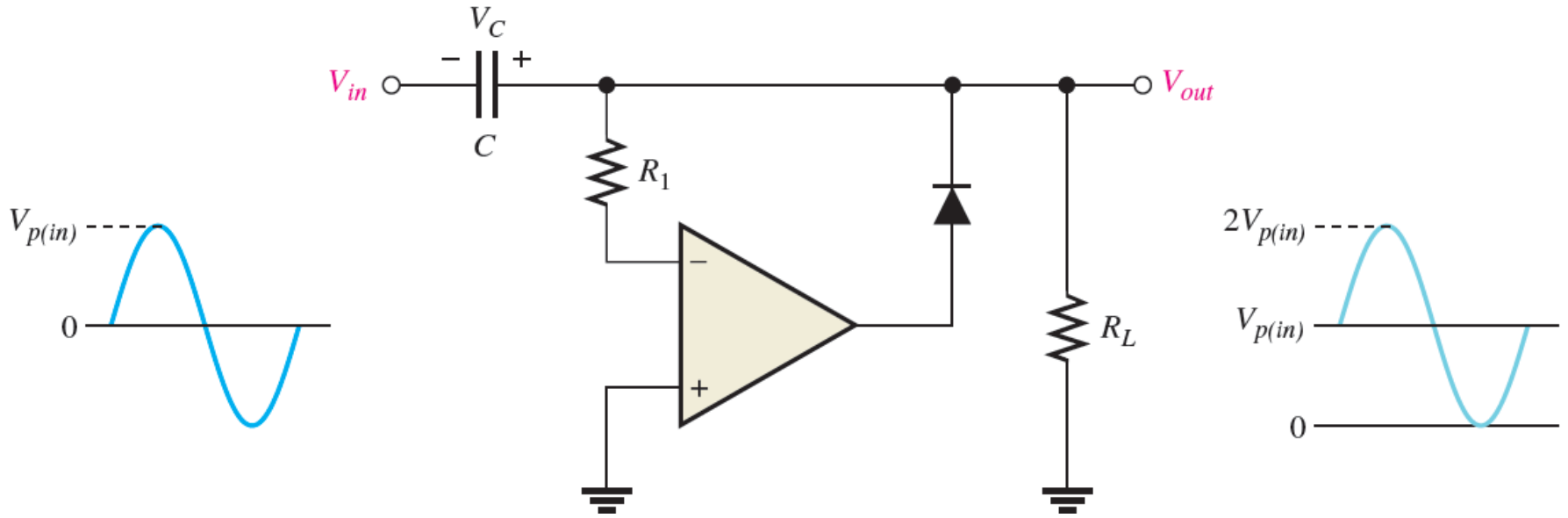

Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

On the first negative half-cycle of the input voltage V_{in}

The differential input is positive, which produces a positive output voltage. Because of the feedback loop, the positive op-amp output voltage forward-biases the diode, allowing the capacitor to charge quickly.

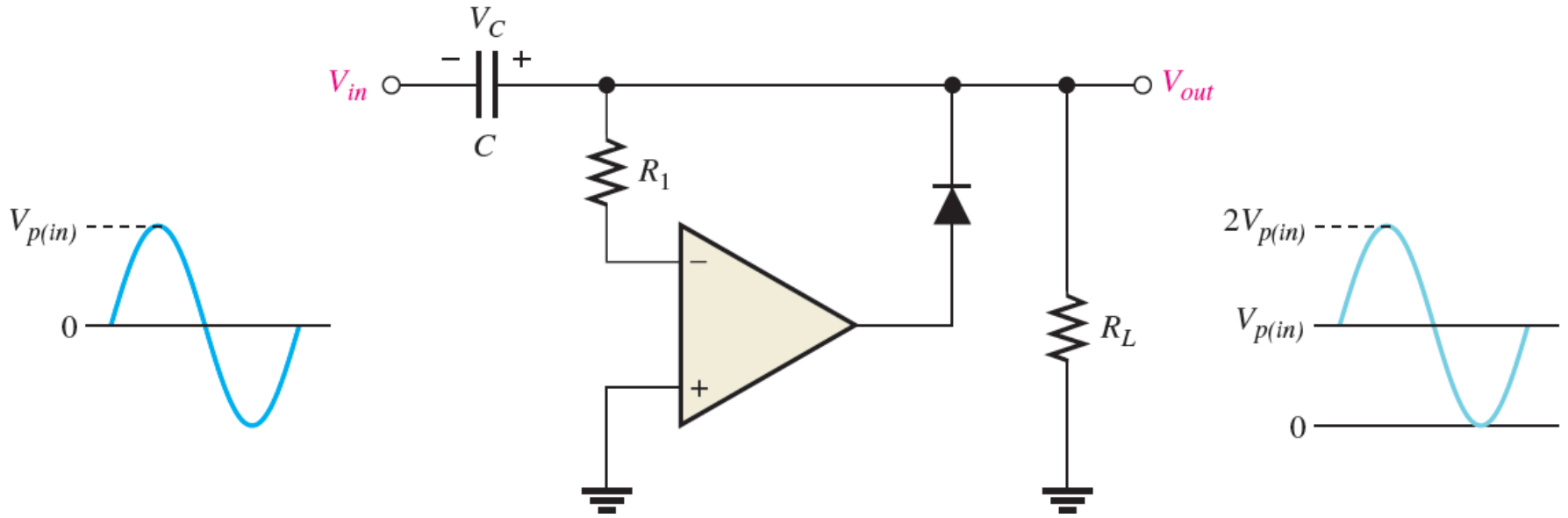

Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

On the first negative half-cycle of the input voltage V_{in}

The maximum voltage across the capacitor occurs at the negative peak of the input with the polarity shown in Fig. 5. This capacitor voltage adds to the input voltage so that the minimum peak of the output voltage, V_{out} is at 0 V, as indicated.

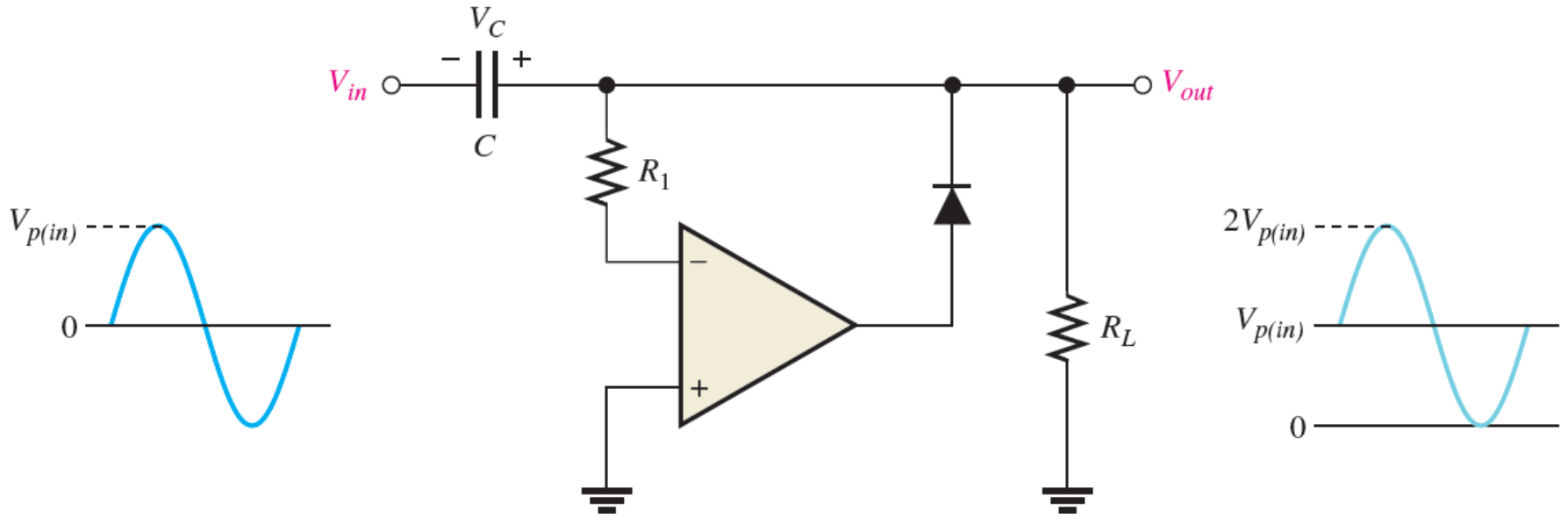

Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

During the time between the minimum output peaks of V_{out} and after the capacitor is charged, the differential input voltage to the op-amp becomes negative. As a result, the output of the op-amp becomes negative and reverse-biases the diode, thus breaking the feedback path. The only change in the capacitor voltage during this time is due to a very small discharge through R_L.

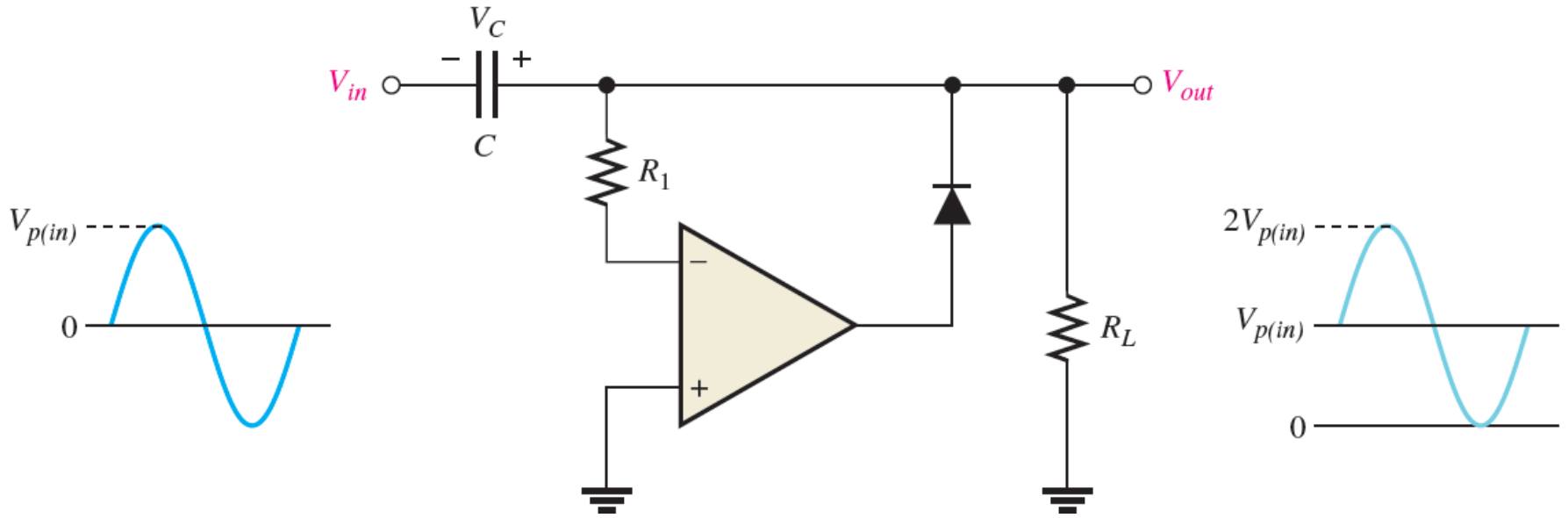

Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

At each minimum peak of the signal, the diode is forward-biased for a very short time to replenish the voltage across the capacitor.

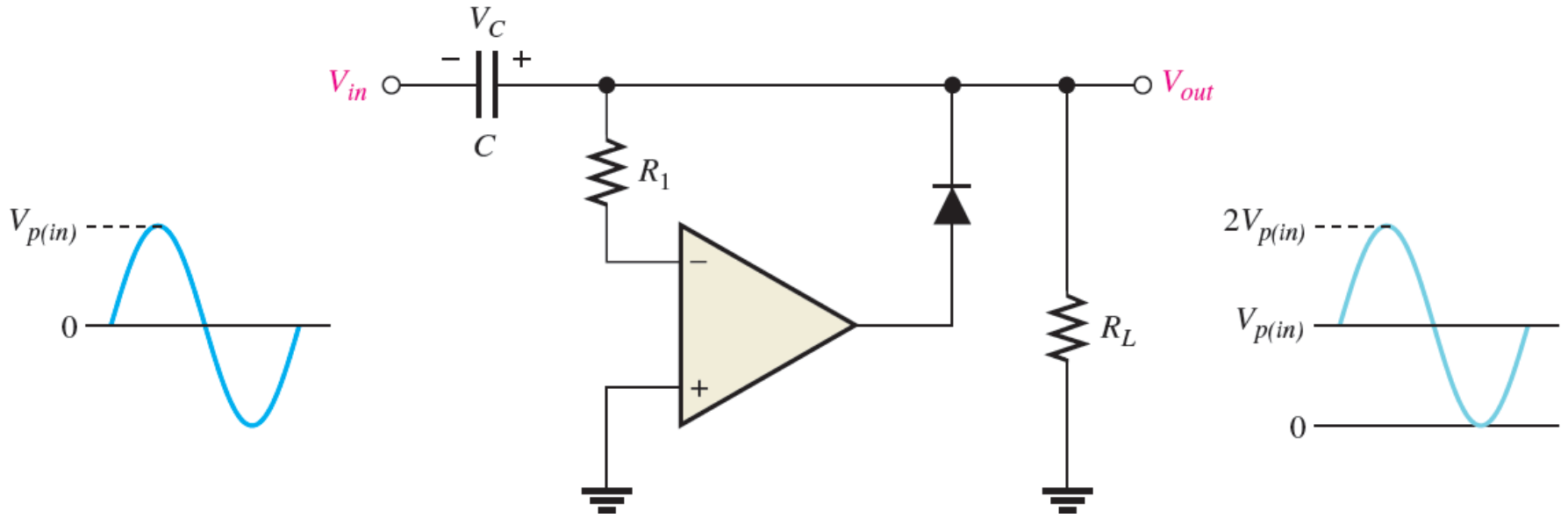

Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

The positive clamper can be converted to a negative clamper by reversing the diode. In this case, the output waveform would occur below 0 V with its maximum peaks at zero, as illustrated in Fig. 6

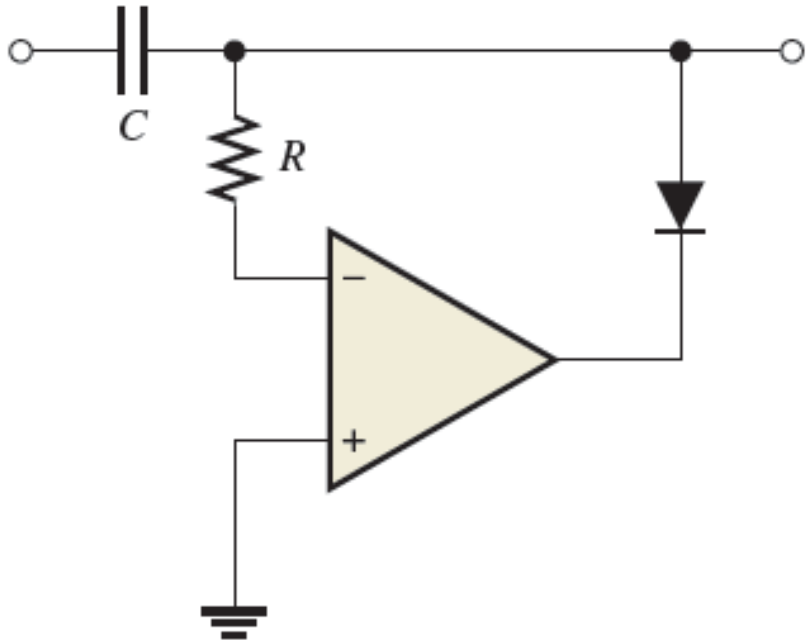

Fig. 6: Active negative clamper.

An Active Clamping Circuit

Also, the clamping level can be changed to a value other than 0 V by connecting a reference voltage source at the input of the op-amp, as shown in Fig. 7.

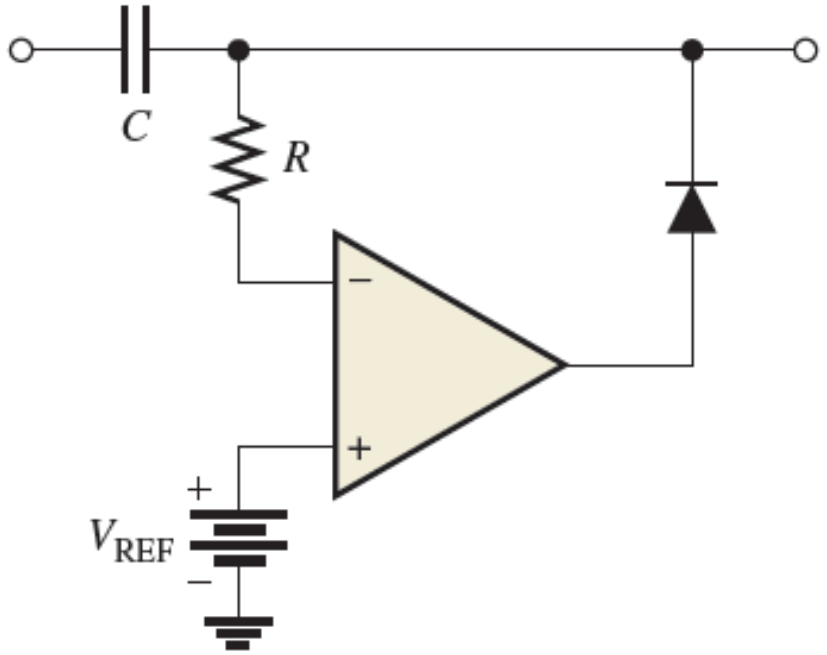

Fig. 7: Active positive clamper with nonzero reference.

An Active Clamping Circuit

Exercise: Determine the output voltage for the clamping circuit in Fig.8 for the input voltage shown.

Solution:

This is a positive clamping circuit and the reference voltage is + 1 V, so the minimum peak value of the output voltage is also +1 V. The voltage is effectively shifted by 3 V, as indicated in the figure.

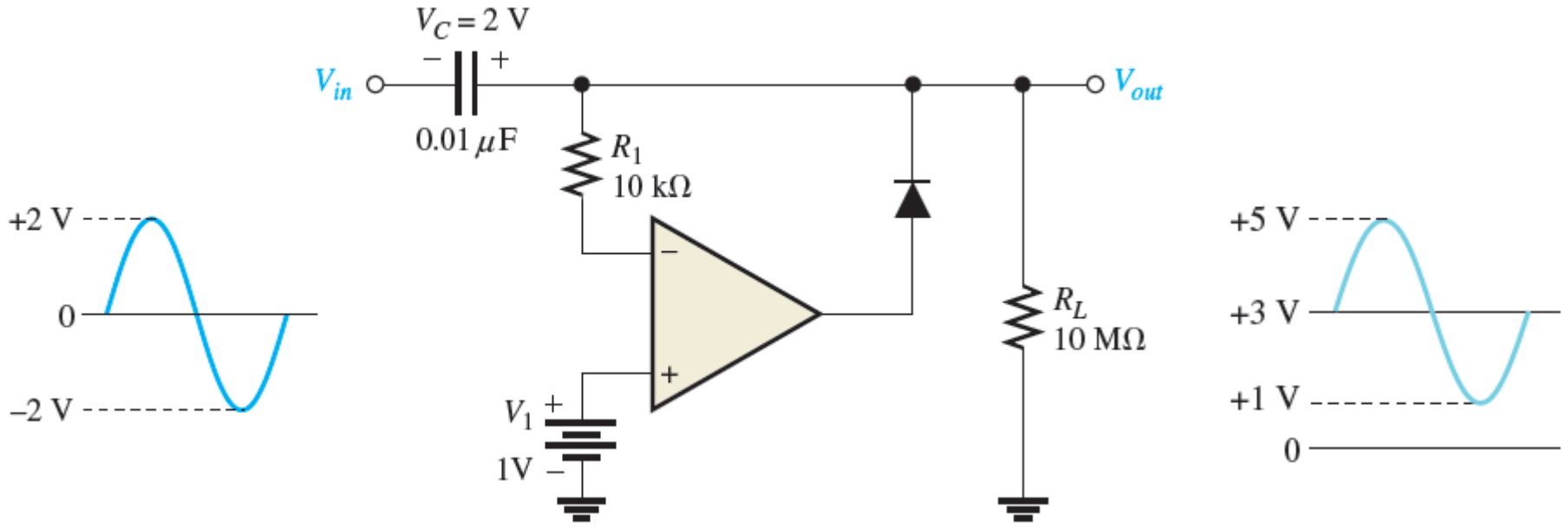

Fig. 8: Active positive clamper with nonzero reference.

An Active Clamping Circuit

Q:

a) Determine the output voltage for the clamping circuit in Fig.9 for the input voltage shown.
b) Determine the time constant for the circuit.
c) Is the clamping circuit below is sufficient if the input frequency is 100 Hz?

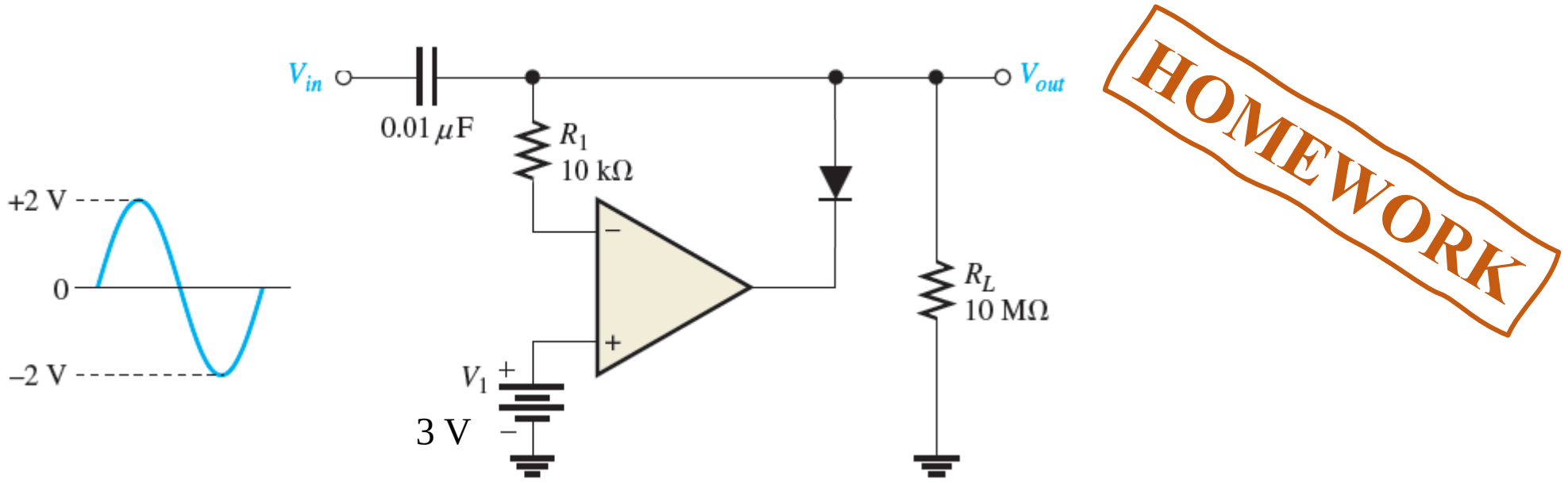

Fig. 9: Active positive clamper with nonzero reference.