JFET Small-Signal Analysis

Common-Source Configuration:

The common-source configuration circuit of Fig. 17-1 includes a source resistor (R_S) that may or may not be bypassed by a source capacitor (C_S) in the ac domain.

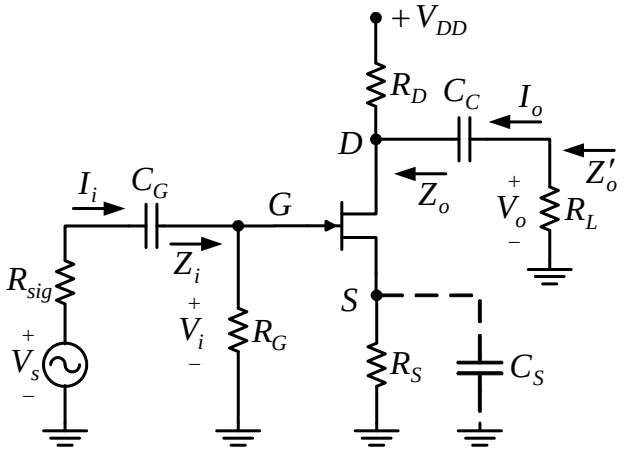

Fig. 17-1

Bypassed (absence of R_S):

For the ac equivalent circuit of Fig. 17-2,

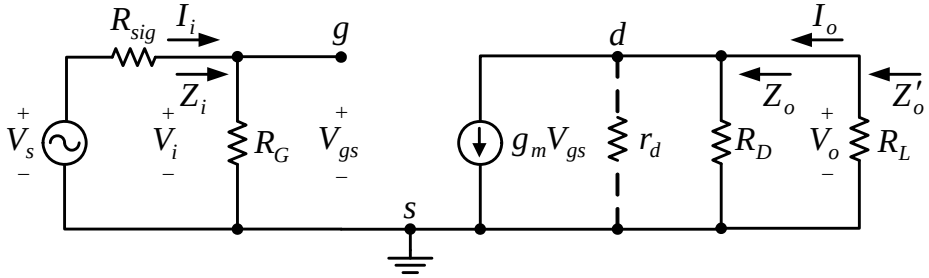

Fig. 17-2

Input impedance:

$$Z_i = R_G$$

Output impedance:

Approximate (neglecting r_d);

$Z_o = R_D$ (for $r_d \geq 10R_D$)

$Z'_o = R_L \| R_D$

Exact (including r_d);

$Z_o = R_D \| r_d$

$Z'_o = R_L \| Z_o = R_L \| R_D \| r_d$

Voltage gain:

Approximate (neglecting r_d);

$V_o = -g_m V_{gs}(R_L \| R_D)$,

$V_{gs} = V_i$,

$$A_v = \frac{V_o}{V_i} = -g_m(R_L \| R_D)$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_v \cdot \frac{Z_i}{Z_i + R_{sig}}$$

Exact (including r_d);

$A_v = -g_m(R_L \| R_D \| r_d)$

Current gain:

$$A_i = \frac{I_o}{I_i} = -A_v \cdot \frac{Z_i}{R_L}$$

Phase relationship:

The negative sign in the resulting equation for A_v reveals that a 180^o phase shift occurs between the input and output signals.

Unbypassed (include of R_S):

For the approximate ac equivalent circuit ($r_d \approx \infty\Omega$) of Fig. 17-3,

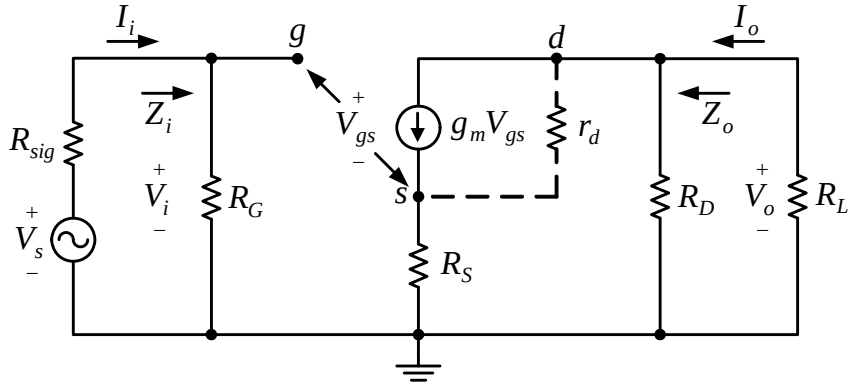

Fig. 17-3

Output impedance:

For $V_i = 0V$, $I_o + I_{R_D} = g_m V_{gs}$, with $V_{gs} = -V_{R_S}\big|_{V_i = 0V} = -(I_o + I_{R_D})R_S$,

so that $I_o + I_{R_D} = -g_m(I_o + I_{R_D})R_S$, or $I_o(1 + g_m R_S) = -I_{R_D}(1 + g_m R_S)$,

and $I_o = -I_{R_D}$.

Since $V_o = -I_{R_D} R_D$, Then $V_o = -(-I_o)R_D = I_o R_D$, and

$$Z_o = \frac{V_o}{I_o} = R_D$$

Voltage gain:

$$V_o = -g_m V_{gs}(R_L \| R_D)$$

$$V_{gs} = V_g - V_s = V_i - g_m V_{gs} R_S \;\Rightarrow\; V_i = (1 + g_m R_S) V_{gs}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m (R_L \| R_D)}{1 + g_m R_S}$$

Common-Drain (Source-Follower) Configuration:

The common-drain (source-follower) configuration circuit is shown in Fig. 17-4.

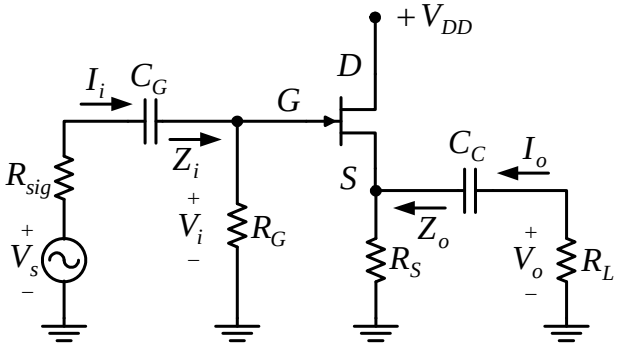

Fig. 17-4

For the ac equivalent circuit of Fig. 17-5,

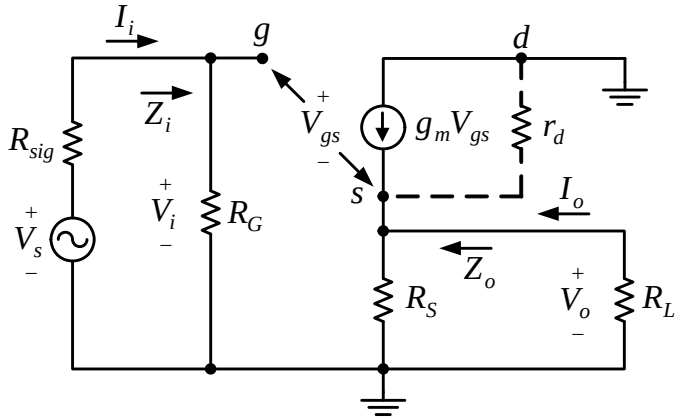

Fig. 17-5

Input impedance:

$$Z_i = R_G \qquad [\textbf{\textit{high}}]$$

Output impedance:

For $V_i = 0V$, $I_o + g_m V_{gs} = I_{r_d} + I_{R_S} = V_o / r_d + V_o / R_S \;\Rightarrow$

$I_o = V_o(1/r_d + 1/R_S) - g_m V_{gs}$, with $V_{gs} = -V_o\big|_{V_i = 0V} \Rightarrow I_o = V_o(1/r_d + 1/R_S + g_m)$,

and $Z_o = V_o / I_o = 1/\left[1/r_d + 1/R_S + 1/(1/g_m)\right]$ =>

$Z_o = r_d \| R_S \| 1/g_m$ [***low***]

$Z_o = R_S \| 1/g_m = \dfrac{R_S}{1 + g_m R_S}$ (for $r_d \geq 10R_S$)

Voltage gain:

$V_o = g_m V_{gs}(R_L \| R_S \| r_d)$,

$V_{gs} = V_g - V_s = V_i - V_o = V_i - g_m V_{gs}(R_L \| R_S \| r_d)$ => $V_i = [1 + g_m(R_L \| R_S \| r_d)]V_{gs}$,

$A_v = \dfrac{V_o}{V_i} = \dfrac{g_m(R_L \| R_S \| r_d)}{1 + g_m(R_L \| R_S \| r_d)}$ [***less than 1***]

$A_v = \dfrac{g_m(R_L \| R_S)}{1 + g_m(R_L \| R_S)}$ (for $r_d \geq 10R_S$)

Phase Relationship:

V_o and V_i are in-phase.

Common-Gate Configuration:

The common-gate configuration circuit is shown in Fig. 17-6.

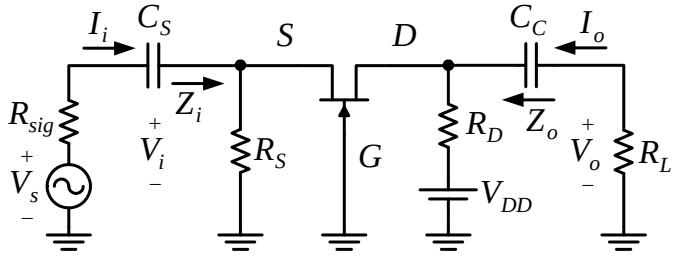

Fig. 17-6

For the approximate ac equivalent circuit ($r_d \approx \infty\Omega$) of Fig. 17-7,

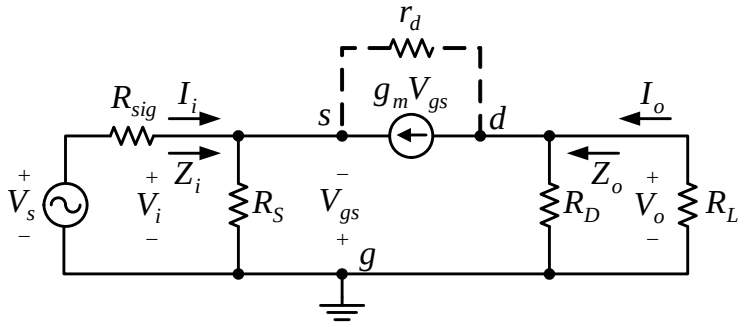

Fig. 17-7

Input impedance:

$$Z_i = R_S \| 1/g_m = \frac{R_S}{1 + g_m R_S} \qquad [\textbf{\textit{low}}] \qquad \text{(Derive)}$$

Output impedance:

$$Z_o = R_D$$

Voltage gain:

$$V_o = -g_m V_{gs}(R_L \| R_D), \text{ and } V_{gs} = -V_i \Rightarrow$$

$$A_v = \frac{V_o}{V_i} = g_m(R_L \| R_D)$$

Phase Relationship:

V_o and V_i are in-phase.

Example 17-1 (Analysis):

For the JFET amplifier circuit of Fig. 17-8 with parameter $g_m = 2.2$ mS, determine: Z_i, Z_o, Z_o', $A_v = V_o/V_i$, $A_i = I_o/I_i$, $A_{v_s} = V_o/V_s$ and V_o. Assume $r_d > 10R_D$.

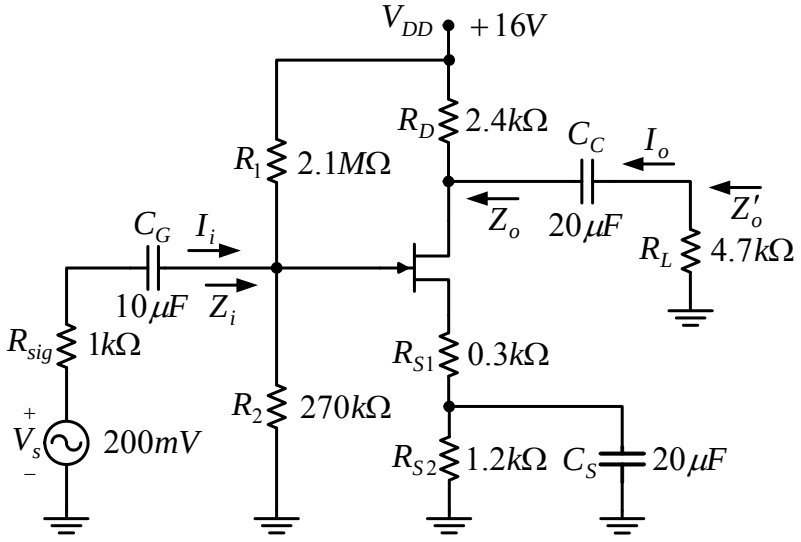

Fig. 17-8

Solution:

$$Z_i = R_1 \| R_2 = 2.1M \| 0.27M = 239k\Omega.$$

$$Z_o = R_D = 2.4k\Omega, \quad Z_o' = R_L \| R_D = 4.7k \| 2.4k = 1.59k\Omega.$$

$$A_v = -\frac{g_m(R_L \| R_D)}{1 + g_m R_{S1}} = -\frac{(2.2m)(1.59k)}{1 + (2.2m)(0.3k)} = -2.11.$$

$$A_i = -A_v \frac{Z_i}{R_L} = -\frac{(-2.11)(239k)}{4.7k} = 107 .$$

$$A_{v_s} = A_v \frac{Z_i}{Z_i + R_{sig}} = \frac{(-2.11)(239k)}{239k + 1k} = -2.10 \approx A_v .$$

$$V_o = A_{v_s} V_s = -2.10(200m) = 420mV .$$

Example 17-2 (Design):

Complete the design of the JFET amplifier circuit shown in Fig. 17-9 to have a voltage gain magnitude of 17.5 dB, using a relatively high level of g_m for this device defined at $V_{GSQ} = V_P/4$. Assume $r_d > 10R_D$.

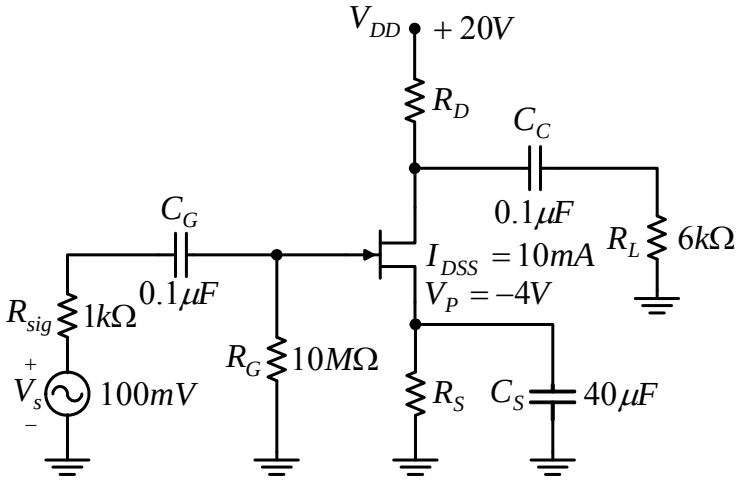

Fig. 17-9

Solution:

$$V_{GSQ} = V_P / 4 = -4/4 = -1V ,$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2(10m)}{4}\left(1 - \frac{-1}{-4}\right) = 3.75mS ,$$

$$G(dB) = 20\log_{10}|A_v| \Rightarrow 17.5 = 20\log_{10}|A_v| \Rightarrow |A_v| = 7.5 ,$$

$$|A_v| = g_m(R_L \| R_D) \Rightarrow 7.5 = 3.75m(6k \| R_D) \Rightarrow R_D = 3k\Omega .$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 = 10m\left(1 - \frac{-1}{-4}\right)^2 = 5.625mA ,$$

$$V_{GSQ} = -I_{DQ}R_S \Rightarrow -1 = -5.625m(R_S) \Rightarrow R_S = 178\Omega .$$

Exercises:

1. For each one of the circuits shown in Fig. 17-10, determine:
   (a) V_{GS}, and g_m. (b) Z_i, and Z_o. (c) $A_v = V_o / V_i$, and $A_i = I_o / I_i$.

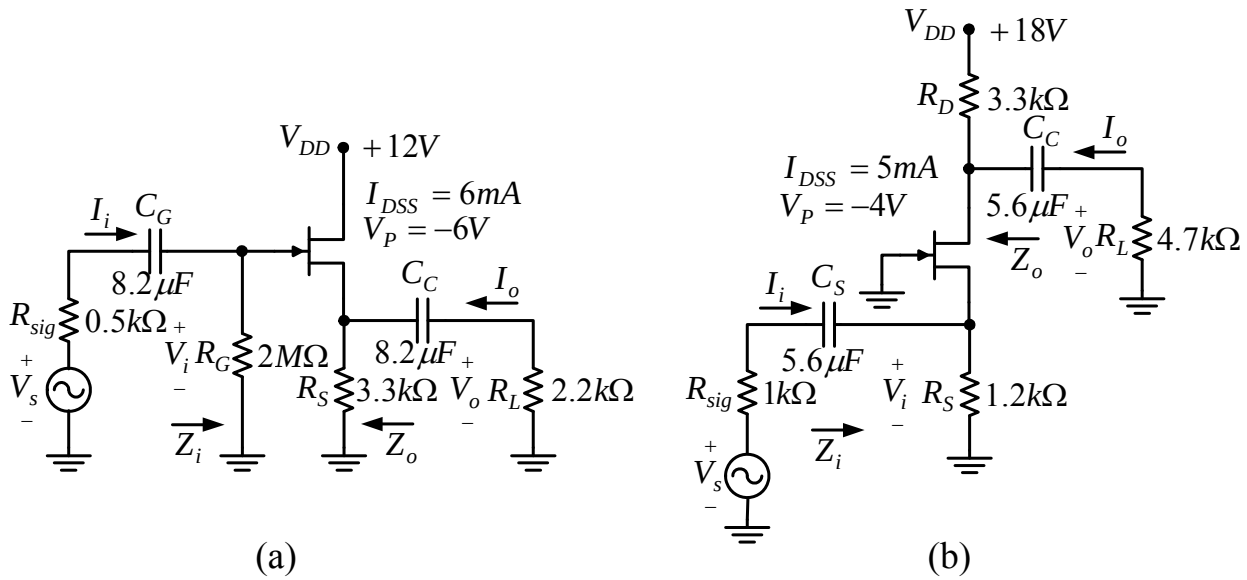

Fig. 17-10

2. Choose the values of R_D, R_S, and R_L for the JFET amplifier circuit of Fig. 17-11 that will result in a gain of 18.062 dB. Assume that I_{DSS} = 8 mA, V_P = −4 V, $r_d \approx \infty$ Ω, V_{DQ}/V_{DD} = 0.375, and I_{DQ}/I_{DSS} = 0.25. Calculate $A_{v_s} = V_o / V_s$, and sketch V_o.

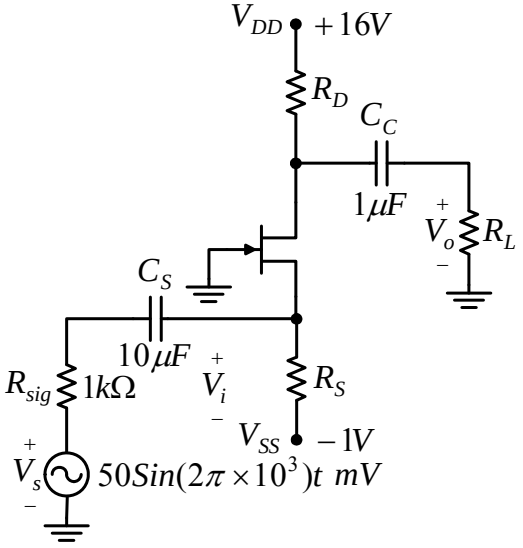

Fig. 17-11