DC Biasing Circuits of JFETs

1. Fixed-Bias Configuration:

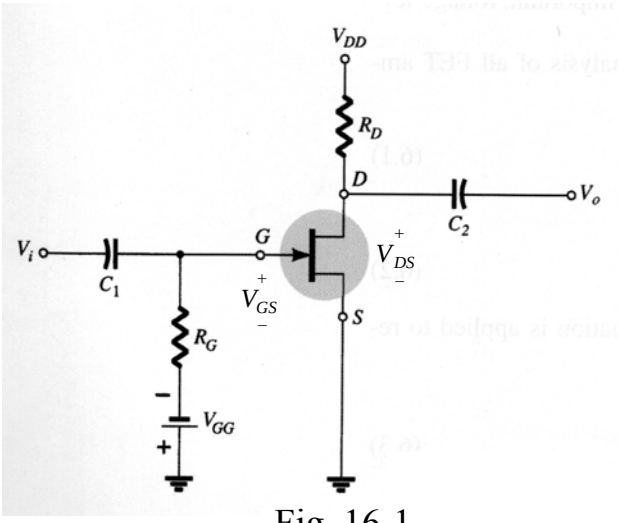

Fig. 16-1

For the circuit of Fig. 16-1,

$$I_G \cong 0A,$$

and $V_{R_G} = I_G R_G = 0V$.

For the input circuit,

$$-V_{GG} - V_{GS} = 0,$$

and $\boxed{V_{GS} = -V_{GG}}$

From Shockley's equation:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

For the output circuit,

$$V_{DD} - I_D R_D - V_{DS} = 0,$$

and $\boxed{V_{DS} = V_{DD} - I_D R_D}$

A graphical analysis is shown in Fig. 16-2.

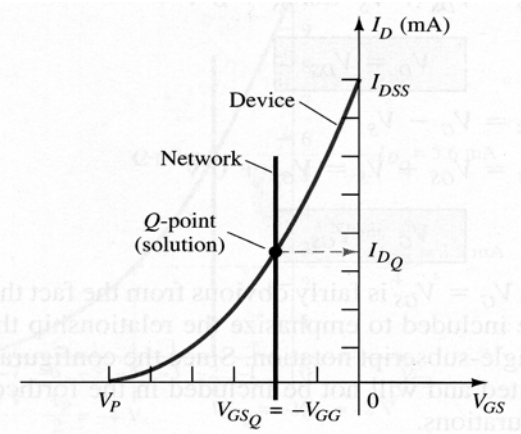

Fig. 16-2

Example 16-1:

For the circuit of Fig. 16-1 with the following parameters: I_{DSS} = 10 mA, V_P = − 8 V, V_{DD} = + 16 V, V_{GG} = 2 V, R_G = 1 MΩ, and R_D = 2 kΩ, determine the following: V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G, and V_S.

Solution:

From Fig. 16-3:

$V_{GSQ} = -V_{GG} = -2V$, and $I_{DQ} = 5.6mA$.

$V_{DS} = V_{DD} - I_D R_D$

$= 16 - (5.6m)(2k) = 4.8V$.

$V_D = V_{DS} = 4.8V$.

$V_G = V_{GS} = -2V$.

$V_S = 0V$.

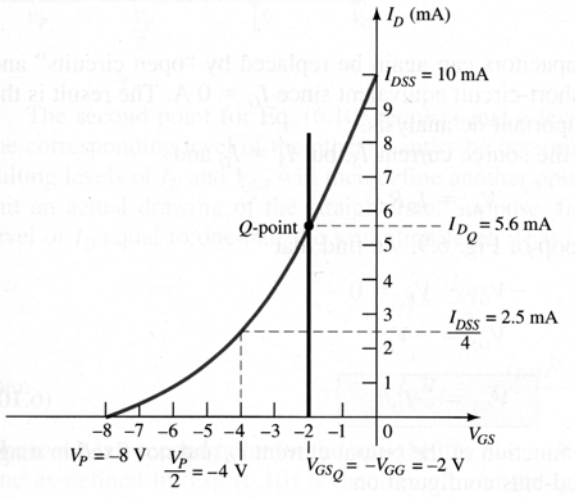

Fig. 16-3

2. Self-Bias Configuration:

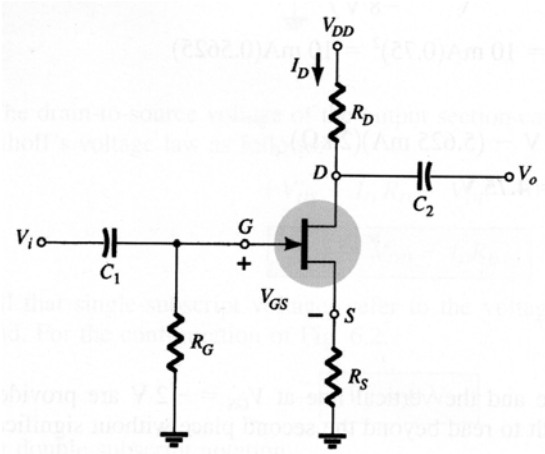

Fig. 16-4

For the circuit of Fig. 16-4,

$I_G \cong 0A,$

and $V_{R_G} = I_G R_G = 0V$.

$I_S = I_D,$

and $V_{R_S} = I_D R_S$.

For the input circuit,

$-V_{GS} - V_{R_S} = 0,$

and $\boxed{V_{GS} = -I_D R_S}$

From Shockley's equation:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

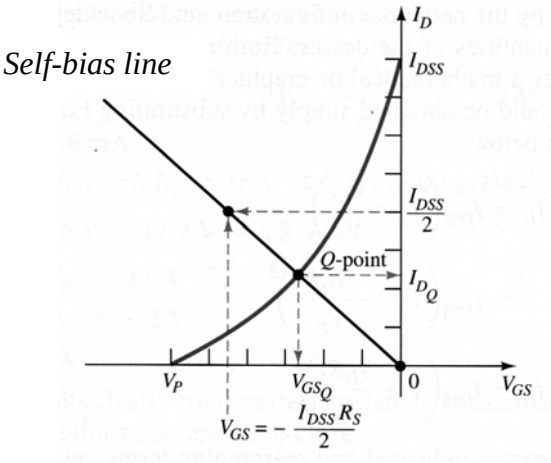

Fig. 16-5

For the output circuit,

$V_{DD} - V_{R_D} - V_{DS} - V_{R_S} = 0,$

and $\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$

A graphical analysis is shown in Fig. 16-5.

Example 16-2:

For the circuit of Fig. 16-4 with the following parameters: I_{DSS} = 8 mA, V_P = − 6 V, V_{DD} = + 20 V, R_G = 1 MΩ, R_S = 1kΩ, and R_D = 3.3 kΩ, determine the following: V_{GSQ}, I_{DQ}, V_{DS}, V_G, V_S, and V_D.

Solution:

Choosing $I_D = 4mA$, we obtain

$V_{GS} = -I_D R_S = -(4m)(1k) = -4V.$

At the *Q*-point (see Fig. 16-6):

$V_{GSQ} = -2.6V$, and $I_{DQ} = 2.6mA$.

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 20 - (2.6m)(1k + 3.3k) = 8.82V.$

$V_G = 0V$, and $V_S = I_D R_S = (2.6m)(1k) = 2.6V.$

$V_D = V_{DD} - I_D R_D = 20 - (2.6m)(3.3k) = 11.42V,$

or $V_D = V_{DS} + V_S = 8.82 + 2.6 = 11.42V.$

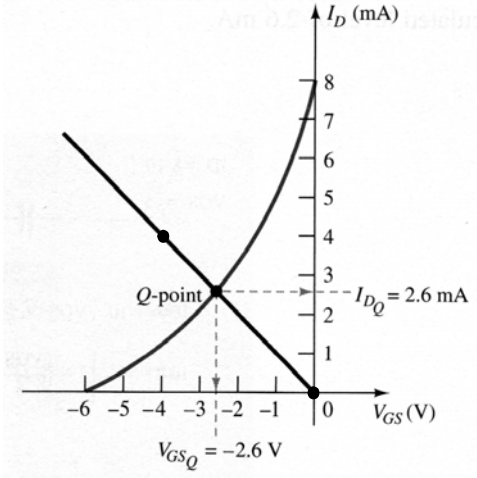

Fig. 16-6

Example 16-3 (Common-Gate Configuration):

For the ***common-gate*** configuration of Fig. 16-7, determine the following: V_{GSQ}, I_{DQ}, V_D, V_G, V_S, and V_{DS}.

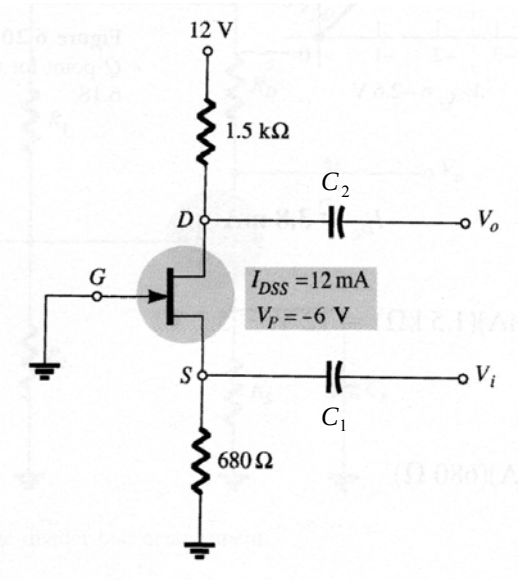

Fig. 16-7

Solution:

Choosing $I_D = 6mA$, we obtain $V_{GS} = -I_D R_S = -(6m)(680) = -4.08V$.
At the *Q*-point (see Fig. 16-8): $V_{GSQ} \cong -2.6V$, and $I_{DQ} \cong 3.8mA$.
$V_D = V_{DD} - I_D R_D = 12 - (3.8m)(1.5k) = 6.3V$.
$V_G = 0V$.
$V_S = I_D R_S = (3.8m)(680) = 2.58V$.
$V_{DS} = V_D - V_S = 6.3 - 2.58 = 3.72V$.

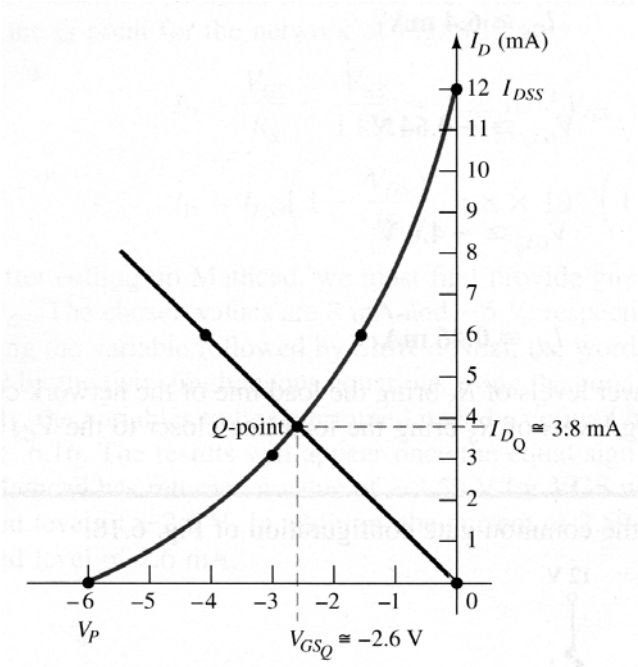

Fig. 16- 8

Example 16-4 (Design):

For the circuit of Fig. 16-9, the levels of V_{DQ} and I_{DQ} are specified. Determine the required values of R_D and R_S.

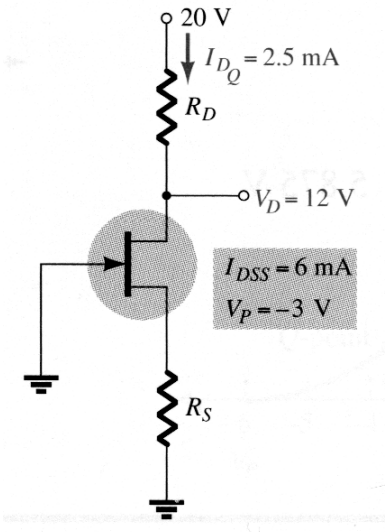

Fig. 16-9

Solution:

$$R_D = \frac{V_{R_D}}{I_{DQ}} = \frac{V_{DD} - V_{DQ}}{I_{DQ}} = \frac{20 - 12}{25m} = 3.2k\Omega .$$

Plotting the transfer curve as shown in Fig. 16-10 and drawing a horizontal line at I_{DQ} = 2.5 mA will result in V_{GSQ} = − 1 V, and applying $V_{GS} = -I_D R_S$ will establish the level of R_S :

$$R_S = \frac{-V_{GSQ}}{I_{DQ}} = \frac{-(-1)}{2.5m} = 0.4k\Omega .$$

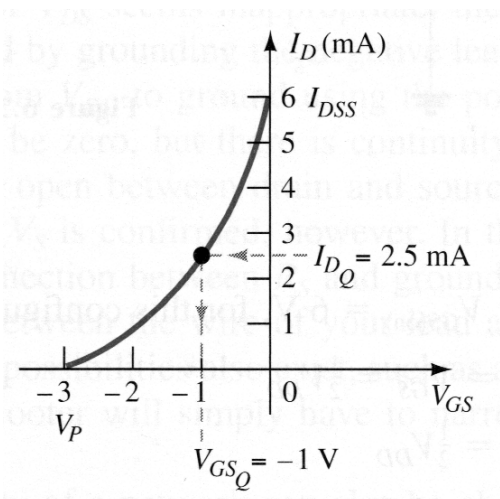

Fig. 16-10

3. Voltage-Divider Bias Configuration:

For the circuit of Fig. 16-11,

$$I_G \cong 0A \;\Rightarrow\; I_{R_1} = I_{R_2},$$

and $$\boxed{V_G = \frac{V_{DD} \cdot R_2}{R_1 + R_2}}.$$

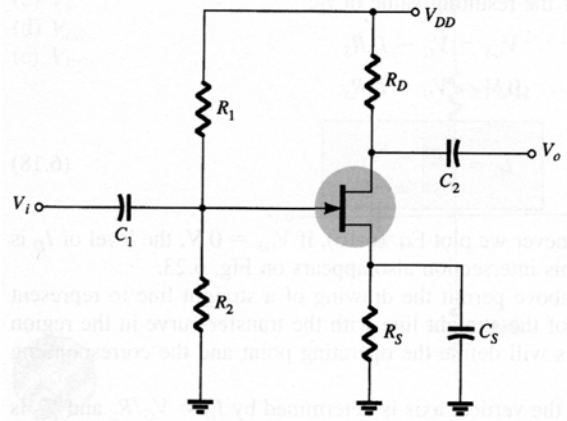

Fig. 16-11

For the input circuit,

$$V_G - V_{GS} - V_{R_S} = 0,$$

$$V_{R_S} = I_S R_S = I_D R_S,$$

and $$\boxed{V_{GS} = V_G - I_D R_S}$$

From Shockley's equation:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

For the output circuit,

$$V_{DD} - V_{R_D} - V_{DS} - V_{R_S} = 0,$$

and $$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

A graphical analysis is shown in Fig. 16-12.

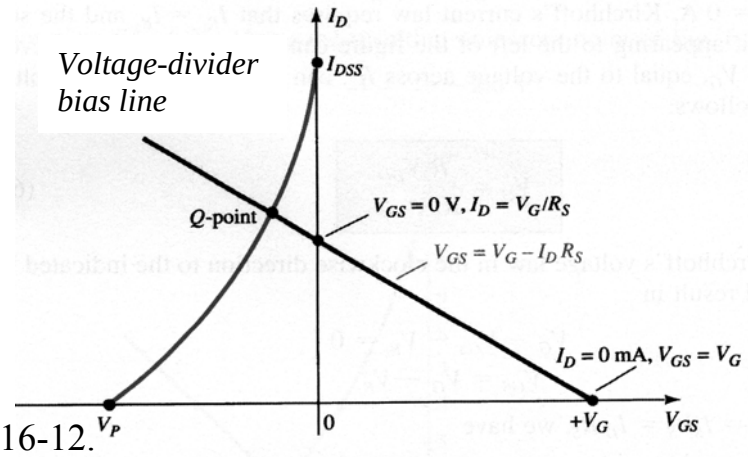

Fig. 16-12

Example 16-5:

For the circuit of Fig. 16-11 with the following parameters: I_{DSS} = 8 mA, V_P = − 4 V, V_{DD} = + 16 V, R_1 = 2.1 MΩ, R_2 = 270 kΩ, R_D = 2.4 kΩ, and R_S = 1.5 kΩ, determine the following: V_{GSQ}, I_{DQ}, V_D, V_S, V_{DS}, and V_{DG}.

Solution:

$$V_G = \frac{V_{DD} \cdot R_2}{R_1 + R_2} = \frac{(16)(270k)}{2.1M + 270k} = 1.82V.$$

$$V_{GS} = V_G - I_D R_S = 1.82 - I_D(1.5k),$$

when $I_D = 0mA$: $V_{GS} = 1.82V$, and

when $V_{GS} = 0V$: $I_D = \frac{1.82}{1.5k} = 1.21mA.$

At the *Q*-point (see Fig. 16-13):

$V_{GSQ} = -1.8V$, and $I_{DQ} = 2.4mA.$

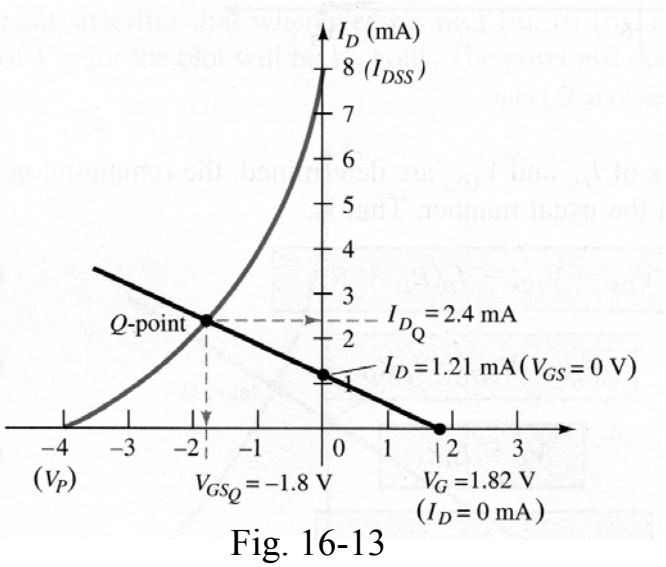

Fig. 16-13

$V_D = V_{DD} - I_D R_D = 16 - (2.4m)(2.4k) = 10.24V$.
$V_S = I_D R_S = (2.4m)(1.5k) = 3.6V$.
$V_{DS} = V_{DD} - I_D(R_D + R_S) = 16 - (2.4m)(2.4k + 1.5k) = 6.64V$,
or $V_{DS} = V_D - V_S = 10.24 - 3.6 = 6.64V$.
$V_{DG} = V_D - V_G = 10.24 - 1.82 = 8.42V$.

Example 16-6 (Two Supplies):

Determine the following for the circuit of Fig. 16-14;
V_{GSQ}, I_{DQ}, V_{DS}, V_D, and V_S.

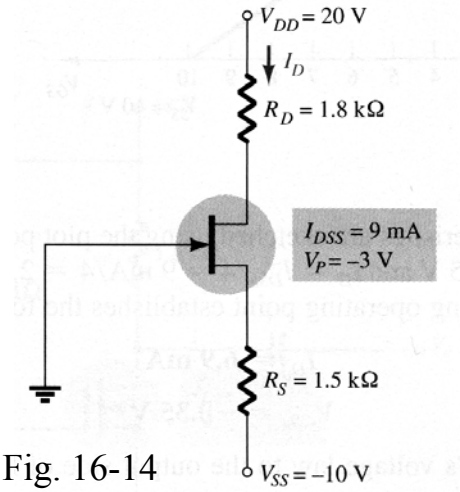

Fig. 16-14

Solution:

For the input circuit of Fig. 16-14,
$-V_{GS} - I_S R_S + V_{SS} = 0$ (KVL)
and $I_G \cong 0A \Rightarrow I_D = I_S$,

$$\boxed{V_{GS} = V_{SS} - I_D R_S}$$

$V_{GS} = 10 - I_D(1.5k)$,
for $I_D = 0mA$; $V_{GS} = 10V$, and
for $V_{GS} = 0V$; $I_D = \dfrac{10}{1.5k} = 6.67mA$.
At the *Q*-point (see Fig. 16-15):
$V_{GSQ} = -0.35V$, and $I_{DQ} = 6.9mA$.
For the output circuit of Fig. 16-14,
$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$,

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)}$$

$V_{DS} = 20 + 10 - (6.9m)(1.8k + 1.5k) = 7.23V$.
$V_D = V_{DD} - I_D R_D = 20 - (6.9m)(1.8k) = 7.58V$.
$V_S = V_D - V_{DS} = 7.58 - 7.23 = 0.35V$.

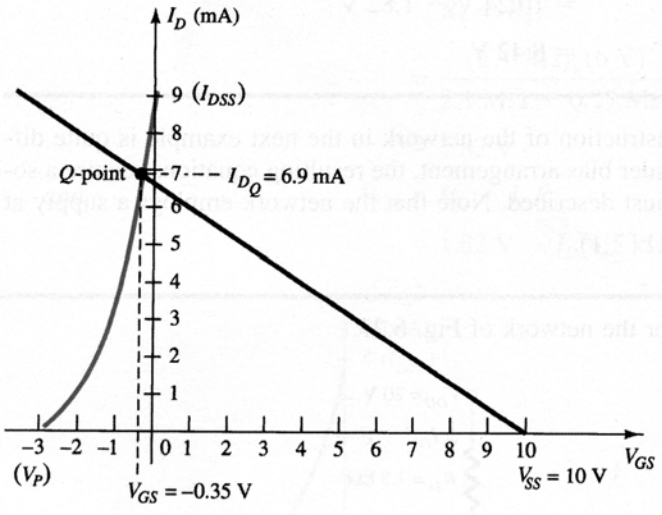

Fig. 16-15

Example 16-7 (p-channel JFET):

Determine V_{GSQ}, I_{DQ}, and V_{DS} for the p-channel JFET of Fig. 16-16.

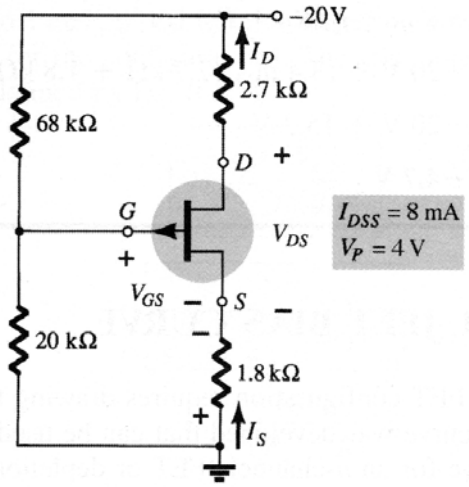

Fig. 16-16

Solution:

$$V_G = \frac{V_{DD} \cdot R_2}{R_1 + R_2} = \frac{(-20)(20k)}{20k + 68k} = -4.55V\,.$$

$V_{GS} = V_G + I_D R_S = -4.55 + I_D(1.8k)$,

when $I_D = 0mA$: $V_{GS} = -4.55V$, and

when $V_{GS} = 0V$: $I_D = \dfrac{-(-4.55)}{1.8k} = 2.53mA$.

At the *Q*-point (see Fig. 16-17): $V_{GSQ} = 1.4V$, and $I_{DQ} = 3.4mA$.

$V_{DS} = -V_{DD} + I_D(R_D + R_S) = -20 + (3.4m)(2.7k + 1.8) = -4.7V$.

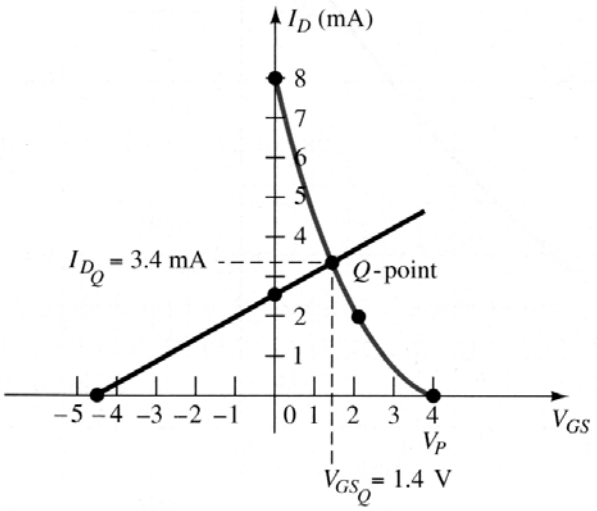

Fig. 16-17

Exercises:

1. For the ***common-drain*** (***source-follower***) configuration of Fig. 16-18, determine the following: V_{GSQ}, I_{DQ}, V_D, V_G, V_S, V_{DG}, and V_{DS}.

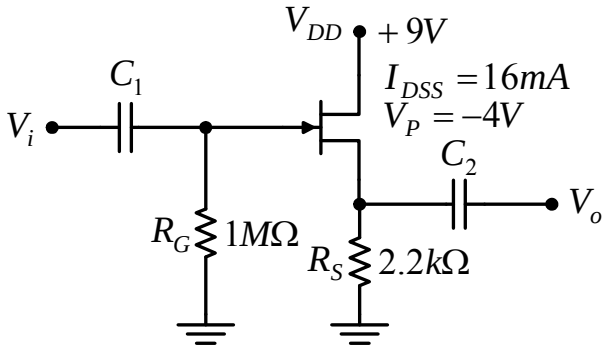

Fig. 16-18

2. For the voltage-divider bias configuration of Fig. 16-19, if V_D = 12 V and $V_{GS} = -2$ V, determine the value of R_S.

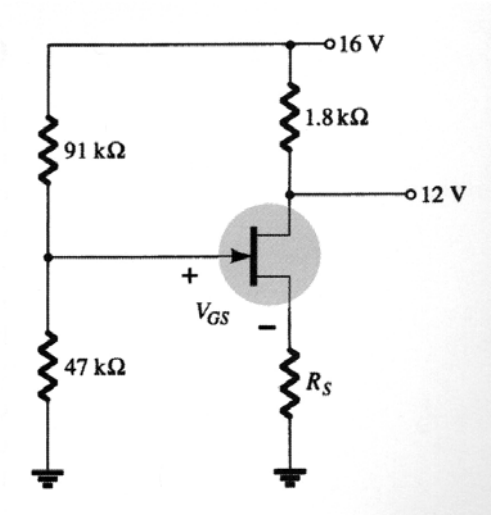

Fig. 16-19