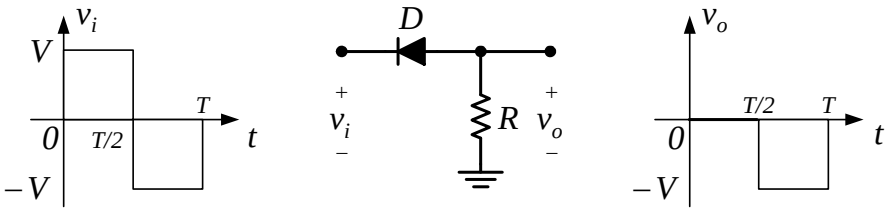
Diode Clipping Circuits

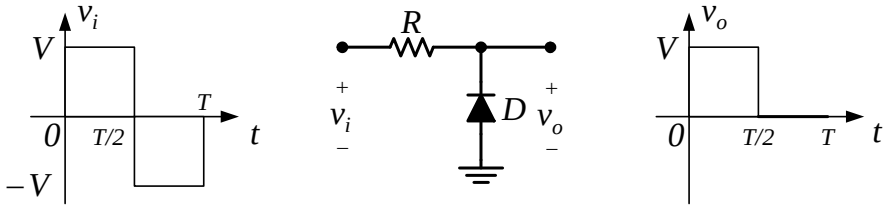
Basic Definition:

There are a variety of diode circuits called ***clippers*** (***limiters*** or ***selectors***) that have the ability to "clip" off a portion of the input signal above (***positive***) or below (***negative***) certain level without distorting the remaining part of the alternating waveform. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: ***series*** and ***parallel***. The series configuration is dined as one where the diode is in series with the load. While the parallel variety has the diode in a branch parallel to the load (see Fig. 3-1).



Simple Series (Positive) Clipper



Simple Parallel (Negative) Clipper

Fig. 3-1

Example 3-1:

Biased Series (Negative) Clipper, see Fig. 3-2.

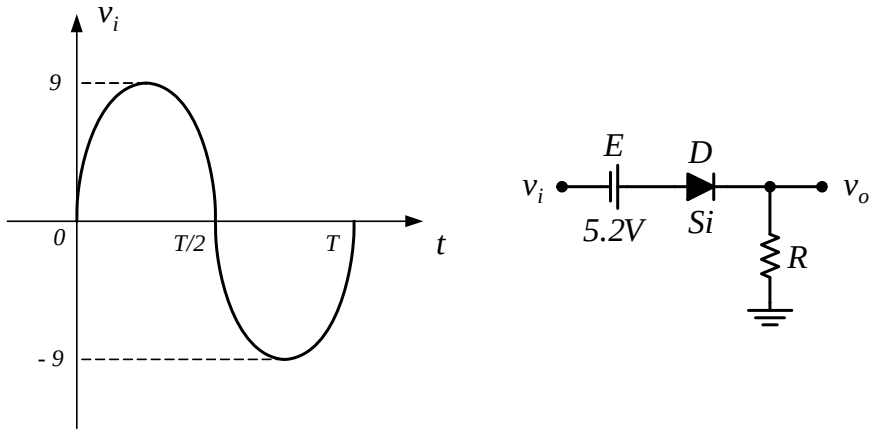
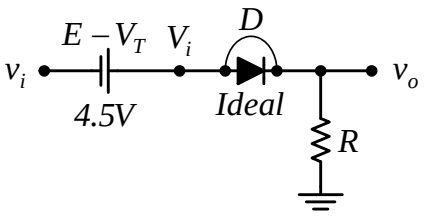
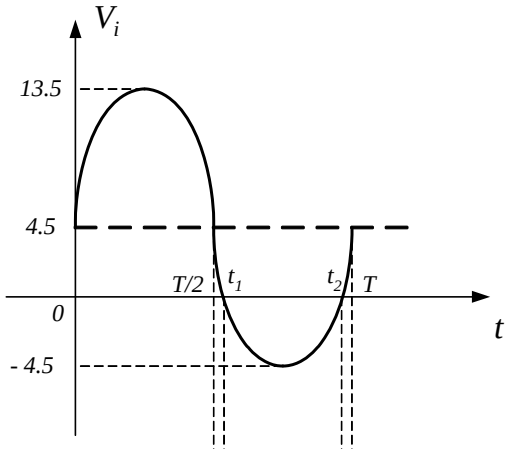
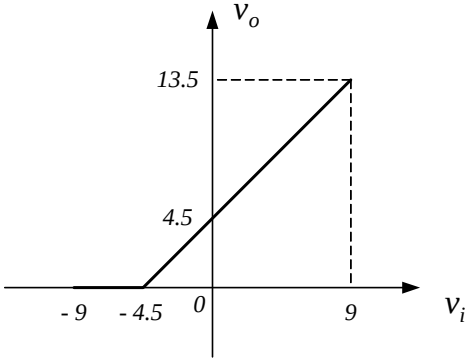


Fig. 3-2



For $t = 0 \rightarrow t_1$ and $t_2 \rightarrow T$; D ON,
and $v_o = v_i + 4.5$ V.
For $t = t_1 \rightarrow t_2$; D OFF,
and $v_o = 0$ V.





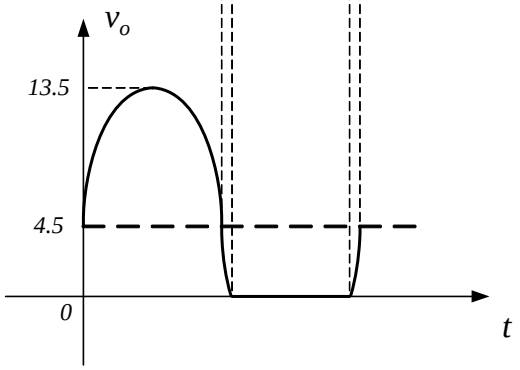
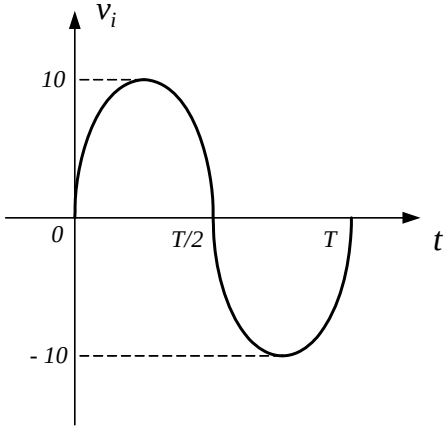


Fig. 3-2 (cont.)

Example 3-2:

Biased Parallel (Positive) Clipper, see Fig. 3-3.



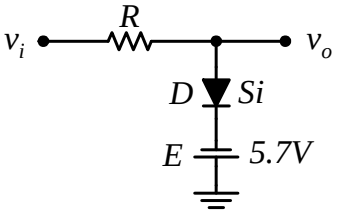
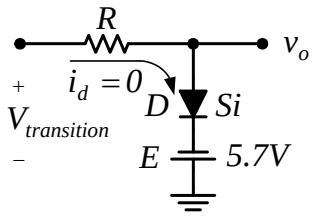
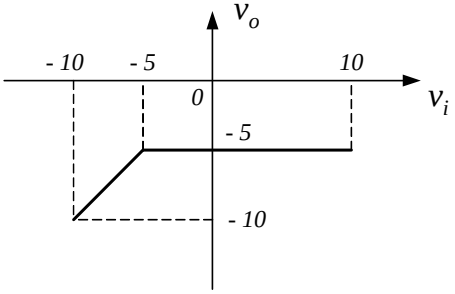


Fig. 3-3



$V_{transition} - i_d R - V_d + E = 0;$
$V_{transition} = 0.7 - 5.7 = -5$ V.
For $t = 0 \rightarrow t_1$ and $t_2 \rightarrow T$; D ON,
and $v_o = -5$ V.
For $t = t_1 \rightarrow t_2$; D OFF,
and $v_o = v_i$.



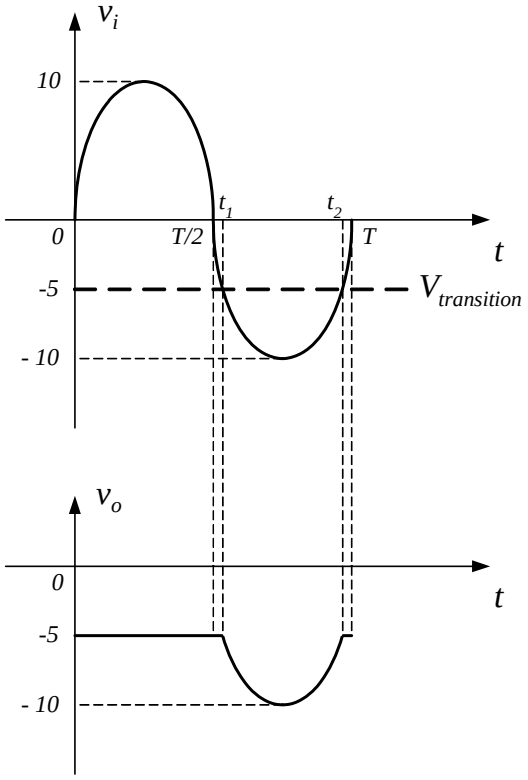


Fig. 3-3 (cont.)

Summary:

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 3-4.

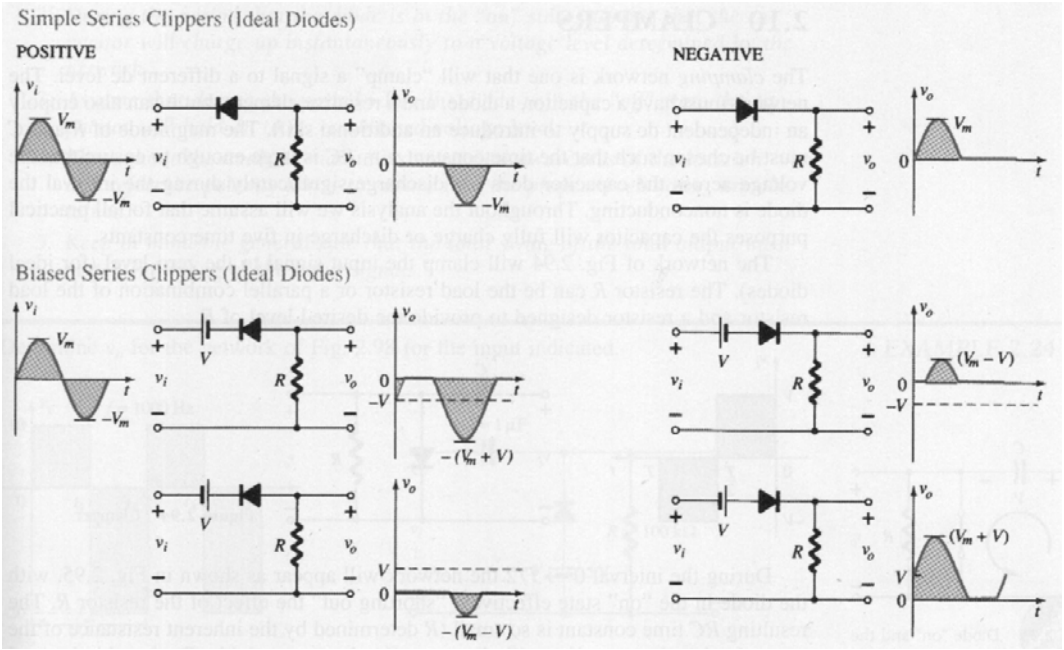


Fig. 3-4

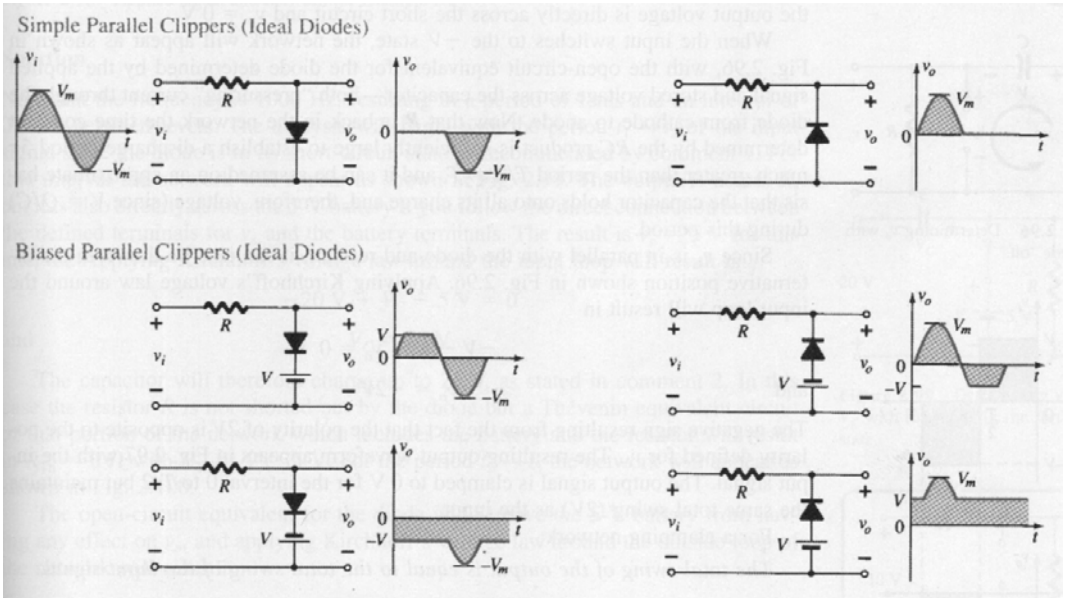


Fig. 3-4 (cont.)

Example 3-3:

Double Diode Series Clipper, see Fig. 3-5.

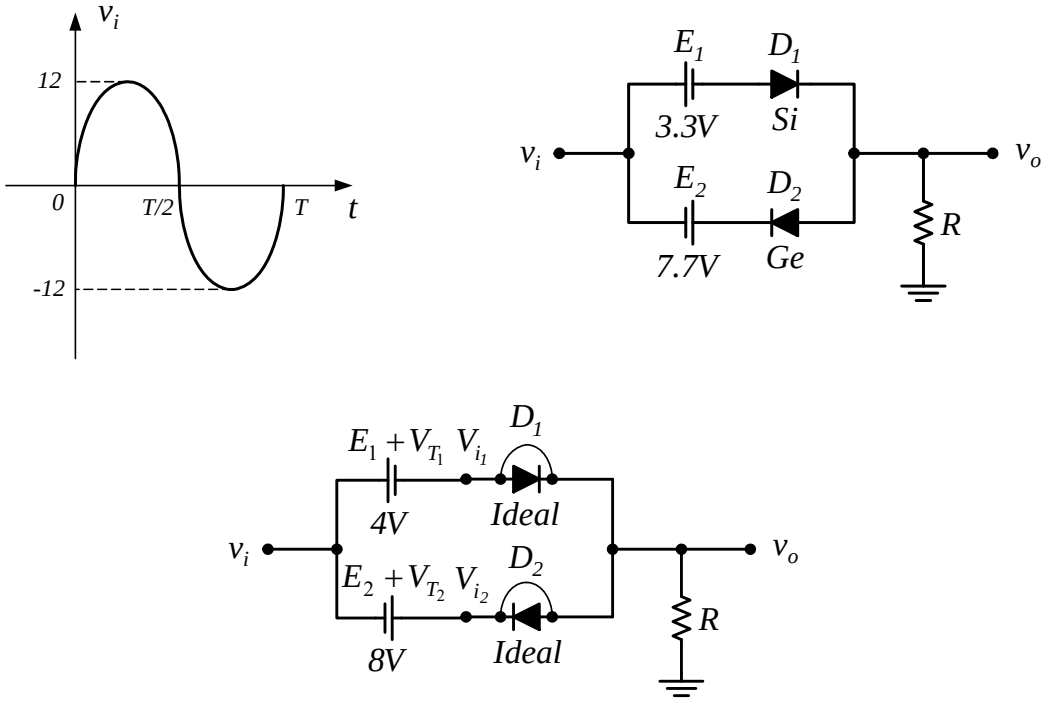
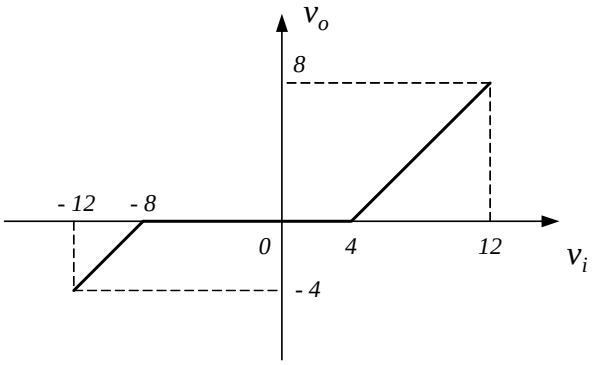


Fig. 3-5

For $t = 0 \rightarrow t_1$, $t_2 \rightarrow t_3$, and $t_4 \rightarrow T$;
both D_1 and D_2 will be OFF,
and $v_o = 0$ V.
For $t = t_1 \rightarrow t_2$; D_1 ON while D_2 OFF,
and $v_o = V_{i_1} = v_i - 4$ V.
For $t = t_3 \rightarrow t_4$; D_1 OFF while D_2 ON,
and $v_o = V_{i_2} = v_i + 8$ V.



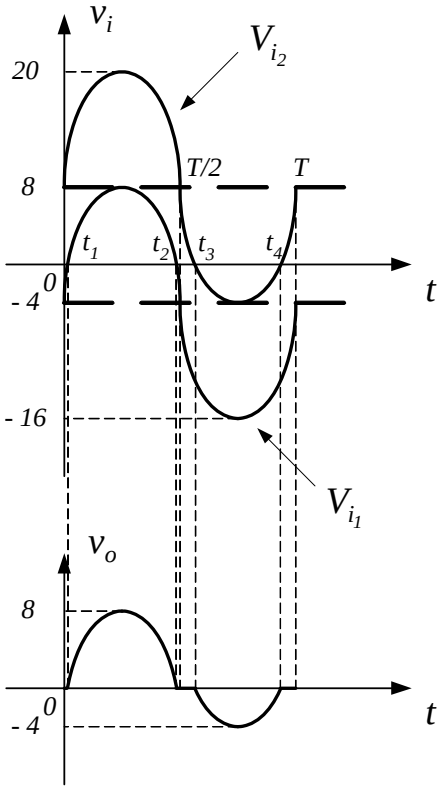
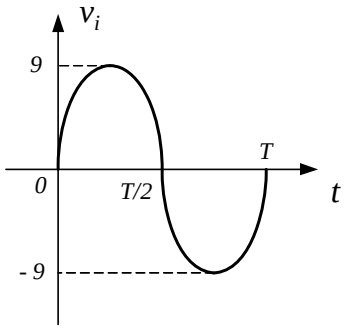
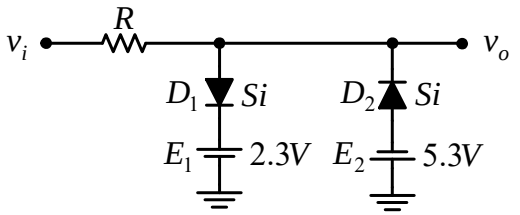


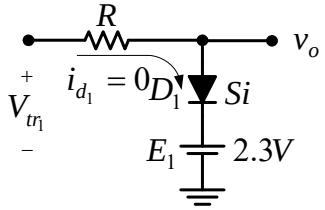
Fig. 3-5 (cont.)

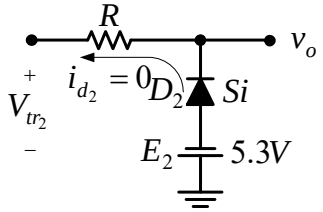
Example 3-4:

Double Diode Parallel Clipper, see Fig. 3-6.







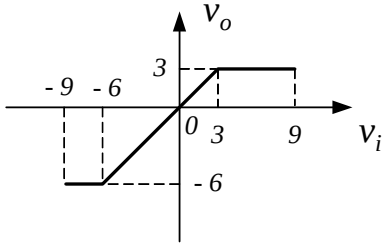


$V_{tr_1} - i_{d_1} R - V_d - E_1 = 0;$
$V_{tr_1} = 0.7 + 2.3 = 3$ V.

$V_{tr_2} + i_{d_2} R + V_d + E_2 = 0;$
$V_{tr_2} = -0.7 - 5.3 = -6$ V.

Fig. 3-6

For $t = 0 \rightarrow t_1$, $t_2 \rightarrow t_3$, and $t_4 \rightarrow T$;
both D_1 and D_2 will be OFF,
and $v_o = v_i$.
For $t = t_1 \rightarrow t_2$; D_1 ON while D_2 OFF,
and $v_o = 3$ V.
For $t = t_3 \rightarrow t_4$; D_1 OFF while D_2 ON,
and $v_o = -6$ V.



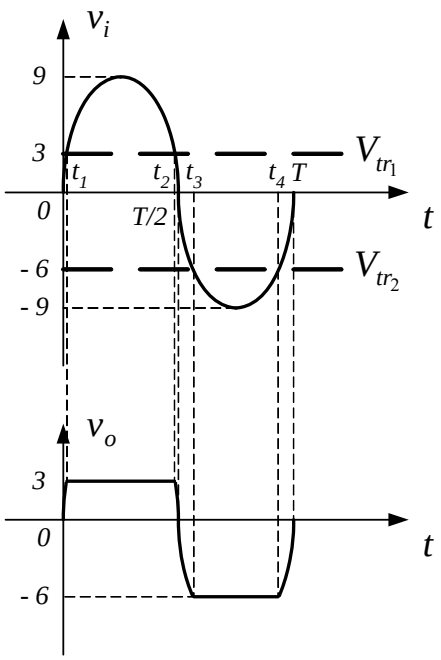
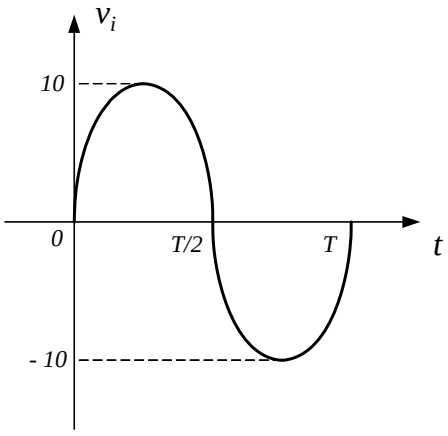


Fig. 3-6 (cont.)

Example 3-5:

Special Type Clipper: A Comparator, see Fig. 3-7.



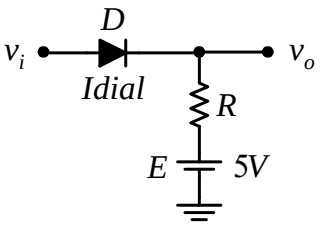
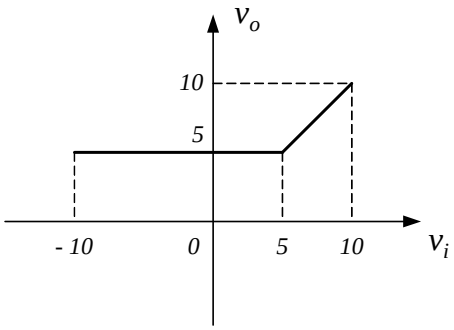


Fig. 3-7

For $t = 0 \rightarrow t_1$ and $t_2 \rightarrow T$; D OFF,
and $v_o = E = 5$ V.
For $t = t_1 \rightarrow t_2$; D ON,
and $v_o = v_i$.



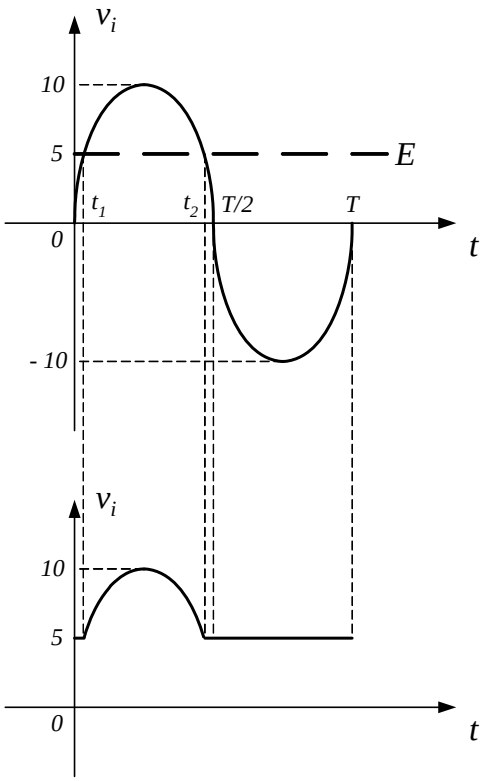
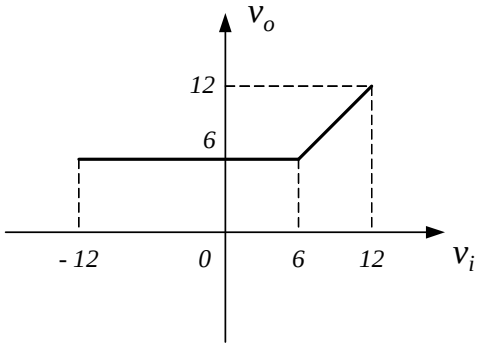


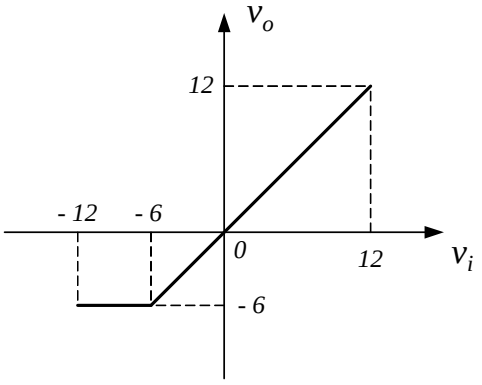
Fig. 3-7 (cont.)

Exercises:

1. Design biased parallel clippers (with silicon diodes) to perform the functions indicated in the transfer characteristics of Fig. 3-8.



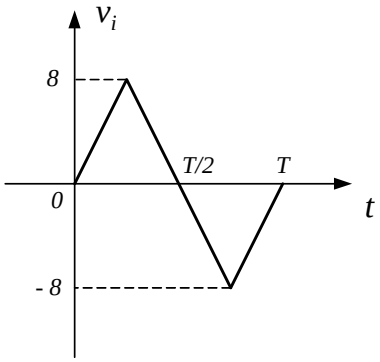
(a)

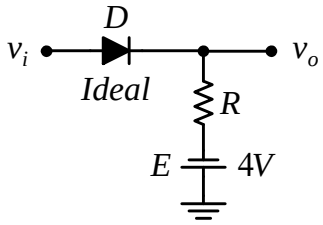


(b)

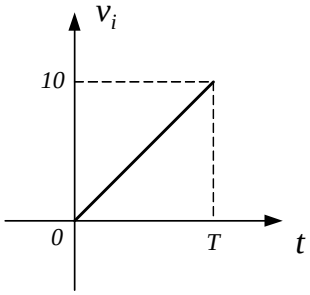
Fig. 3.8

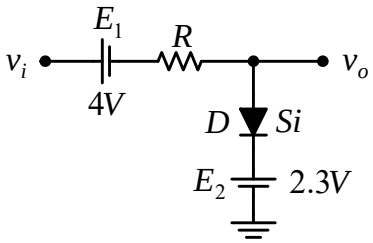
2. Sketch the output voltage (v_o) and the transfer characteristics (v_o against v_i) for each circuit of Fig. 3-9 for the input (v_i) shown.



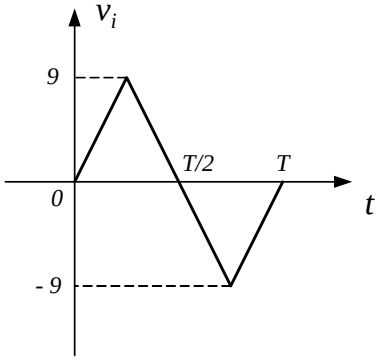


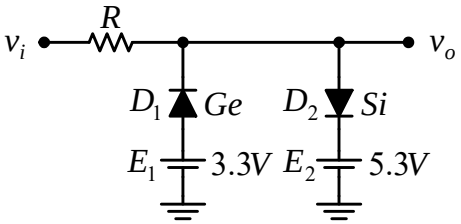
(a)



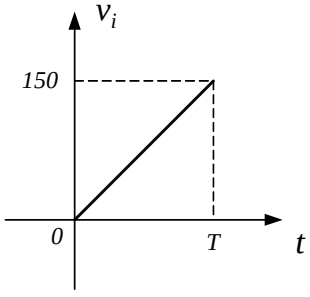


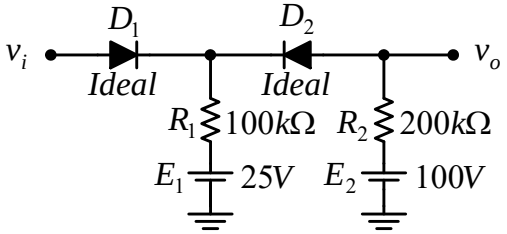
(b)





(c)





(d)

Fig. 3-9

Diode Clamping Circuits

Basic Definition:

The clamping circuit (***clamper***) is one will "clamp" a signal to a different dc level. The circuit must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval $(T/2)$ the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants. Therefore, the condition required for the capacitor to hold its voltage during the discharge period between pulses of the input signal is

$$\boxed{5\tau = 5RC >> \frac{T}{2} = \frac{1}{2f}} \qquad [4.1]$$

Example 4-1:

Determine the output (v_o) for the circuit of Fig. 4-1 for the input (v_i) shown.

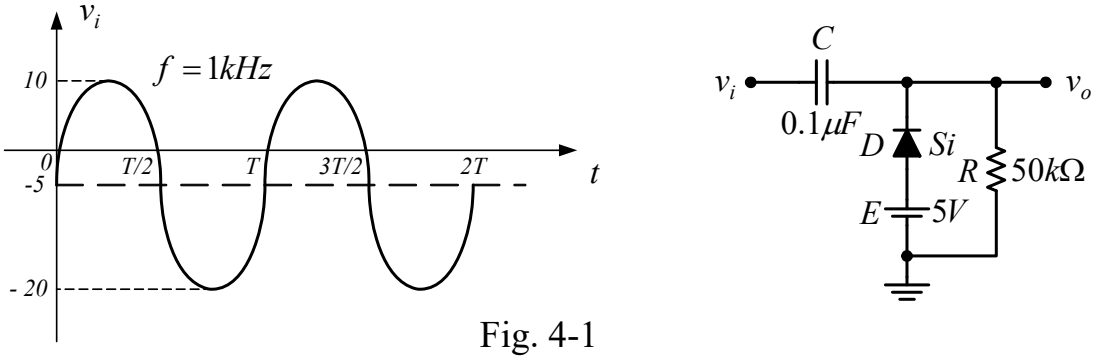


Fig. 4-1

***Solution*:**

The analysis of clamping circuits are started by considering that the part of the input signal that will forward bias the diode. For the circuit of Fig. 4-1, the diode is forward bias ("on" state) during the negative half period of the input signal (v_i) and the capacitor will charge up instantaneously to a voltage level determined by the circuit of Fig. 4-2.

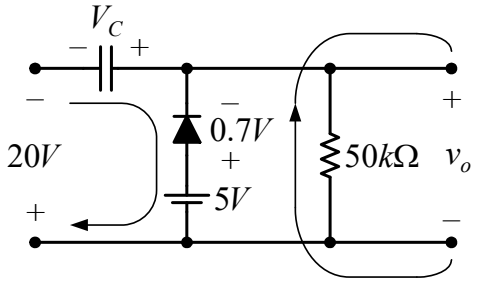


Fig. 4-2

For the input section KVL will result in

$$-20 + V_C + 0.7 - 5 = 0 \quad \Rightarrow \quad V_C = 24.3 \text{ V}.$$

The output voltage (v_o) can be determined by KVL in the output section

$$+5 - 0.7 - v_o = 0 \quad \Rightarrow \quad v_o = 4.3 \text{ V}.$$

Now check that the capacitor will hold on or not its establish voltage level during the period (positive half period in case of Example 4-1) when the diode is in the "off" state (reverse bias). The total time constant 5τ of the discharging circuit of Fig. 4-3 is determined by the product $5RC$ and has the magnitude

$$5\tau = 5RC = 5\,(50\times10^3)\,(0.1\times10^{-6}) = 25 \text{ ms}.$$

The frequency (f) is 1 kHz, resulting in a period of 1 ms and an interval of 0.5 ms between levels, that is

$$T/2 = 1/(2f) = 1/(2 \times 1\times10^3) = 0.5 \text{ ms}.$$

We find that

$$5\tau >> T/2 \quad (25\text{ms} / 0.5\text{ms} = 50 \text{ times}).$$

So that, it is certainly a good approximation that the capacitor will hold its voltage (24.3 V) during the discharge period between pulses of the input signal.

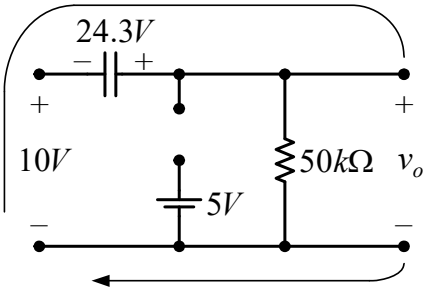


Fig. 4-3

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying KVL around the outside loop of circuit will result in

$$+10 + 24.3 - v_o = 0 \quad \Rightarrow \quad v_o = 34.3 \text{ V}.$$

The resulting output appears in Fig. 4-4, where the input and the output swing are the same.

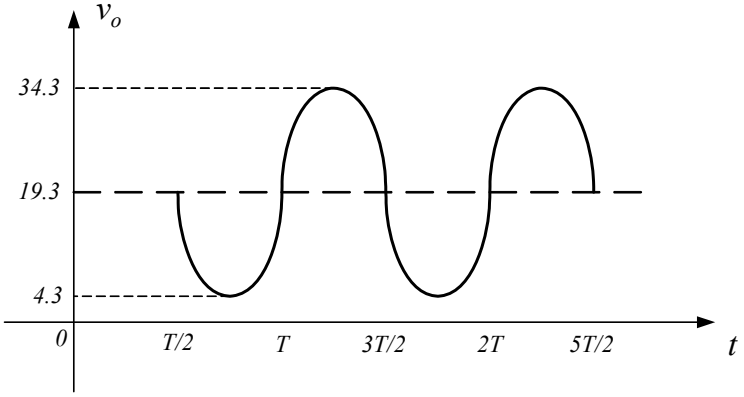


Fig. 4-4

Example 4-2:

Using silicon diode, design a clamper circuit that will produce output $v_o = 10Sin\omega t - 5$ V when the input is $v_i = 10Sin\omega t + 5$ V. Draw the circuit diagram and the input and output signals.

Solution:

From the input (v_i) and output (v_o) signals, we have a negative biased clamper. Therefore, the diode is forward bias ("on" state) during the positive half period of the input signal (v_i). The output voltage (v_o) at this positive period can be determined by KVL in the output section of the circuit shown in Fig. 4-5.

$E + 0.7 - v_o = 0 \quad => \quad E = 5 - 0.7 = 4.3$ V.

For the input section KVL will result in

$15 - V_C - 5 = 0 \quad => \quad V_C = 10$ V.

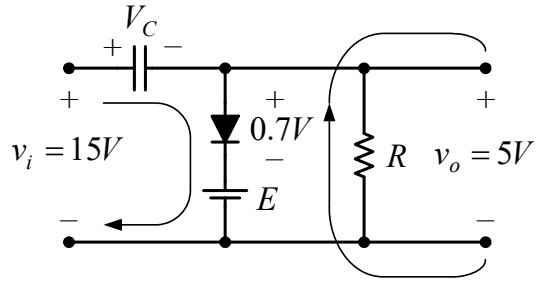


Fig. 4-5

The circuit diagram and the input and output signals are shown in Fig. 4-6.

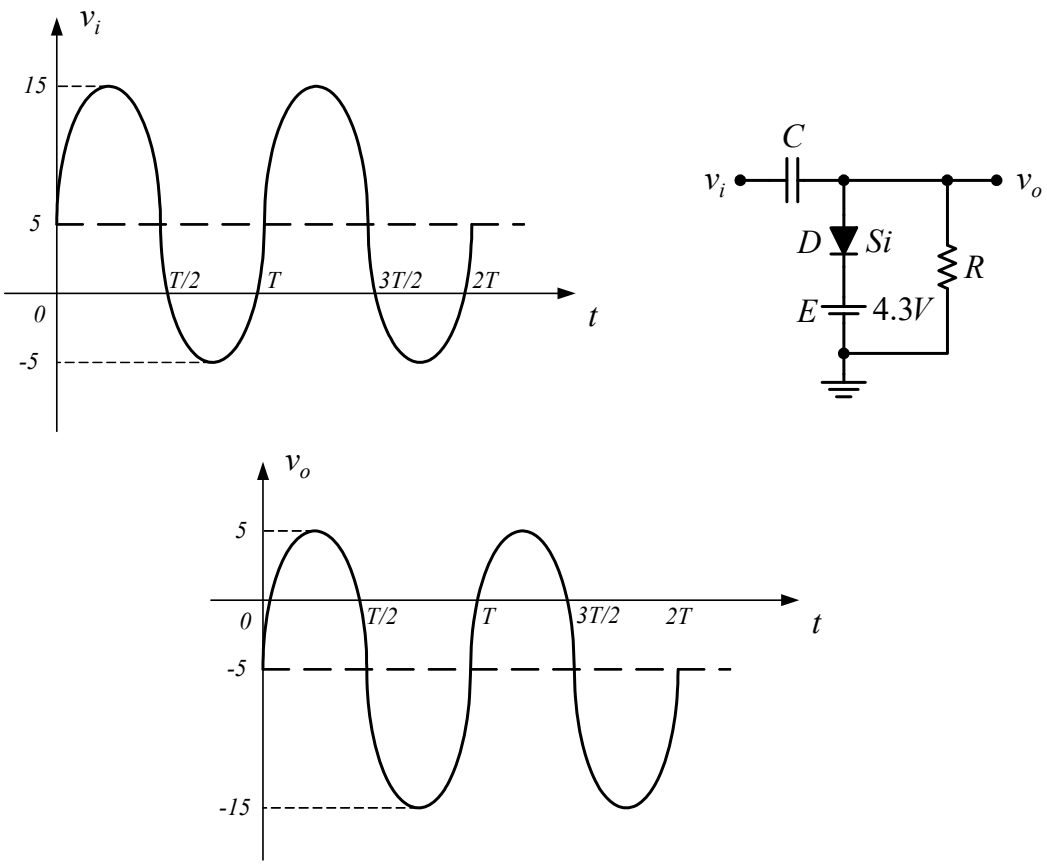
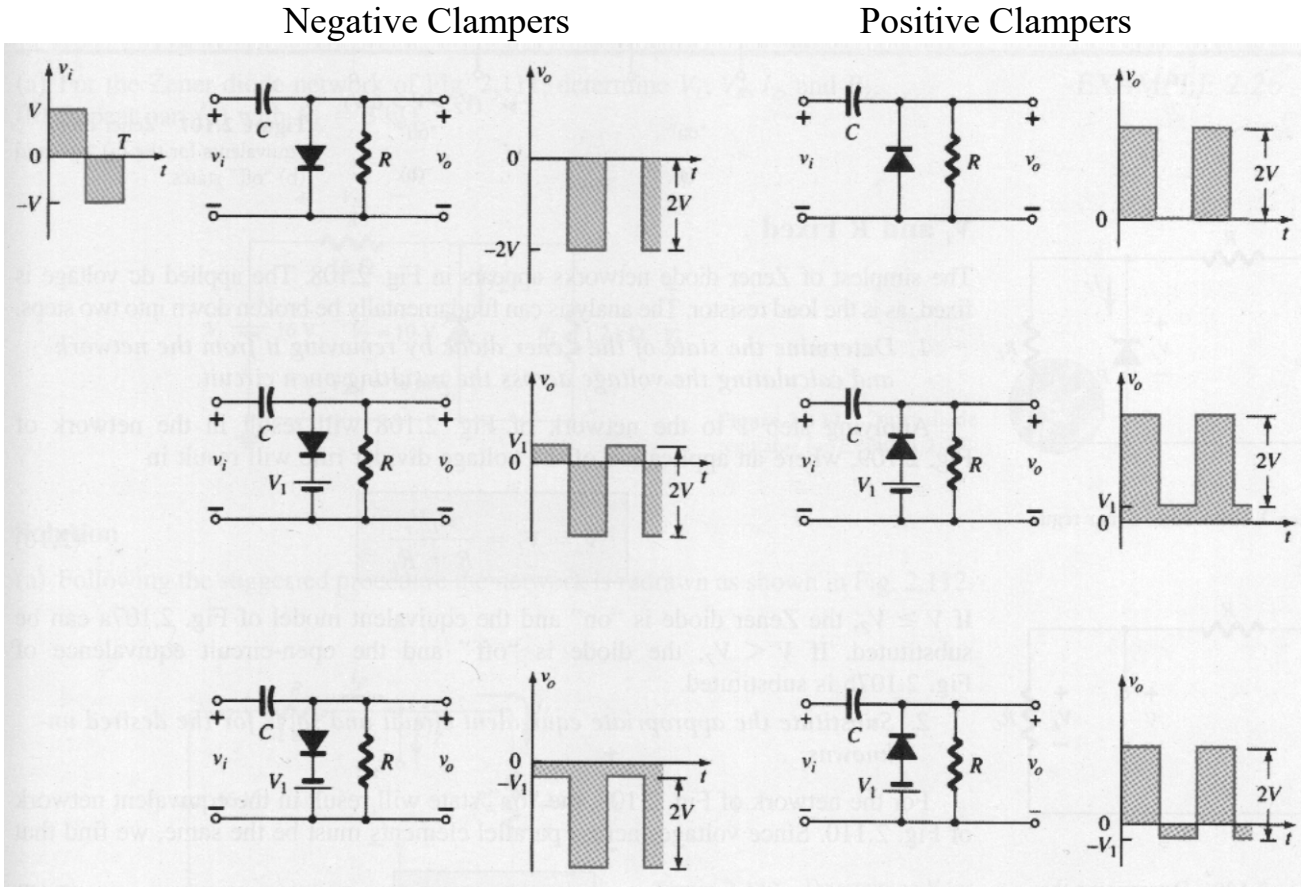


Fig. 4-6

Summary:

A number of clamping circuits and their effect on the square-wave input signal are shown in Fig. 4-7.



Clampers with ideal diodes and $5\tau = 5RC >> T/2$

Fig. 4-7

Exercise:

Sketch the output (v_o) for the circuit of Fig. 4-8 for the input (v_i) shown. Assume ideal diodes.

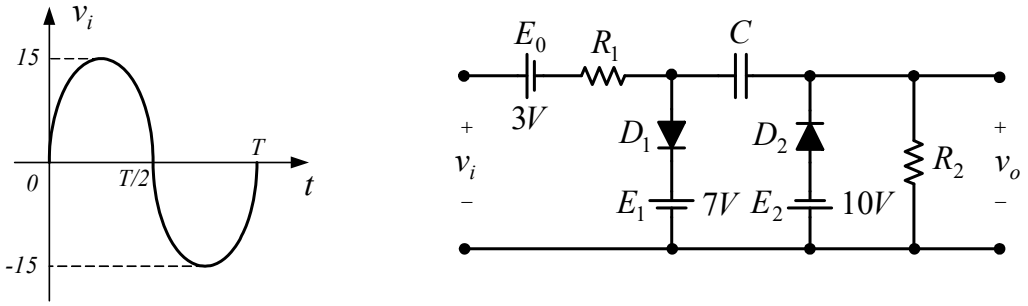


Fig. 4-8