عنوان المحاضرة:

8085 IO / M addressing, Machine Cycle & Bus Timing

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8085 memory addressing, I/O addressing

8085 instructions can be classified in following addressing modes:

- **Register Addressing mode**

Instructions which have their operands in registers only e.g. MOV, ADD, SUB, ANA, ORA, XRA etc.

- **Immediate Addressing mode**

Instructions in which operand immediately follows the op-code e.g. MVI, LXI, ADI, SUI, ANI, ORI etc.

- **Direct Addressing mode**

Instructions have their operands in memory and the 16-bit memory address is specified in the instruction e.g. LDA, STA, LHLD, SHLD etc.

8085 memory addressing, I/O addressing

- **Register Indirect Addressing mode**

Instructions have their operand in memory and the 16-bit memory address is specified in a register pair e.g. LDAX, STAX, PUSH, POP etc.

- **Implicit Addressing mode**

These instruction have their operand implied in the op-code itself e.g. CMA, CMC, STC etc.

8085 machine cycle & bus timing

1. Clock cycle

- The speed of a computer processor, or CPU, is determined by the clock cycle, which is the amount of time between two pulses of an oscillator. Generally speaking, the higher number of pulses per second, the faster the computer processor will be able to process information. The clock speed is measured in Hz, typically either megahertz (MHz) or gigahertz (GHz). For example, a 3GHz processor performs 3,000,000,000 clock cycles per second.
- Computer processors can execute one or more instructions per clock cycle, depending on the type of processor. Early computer processors and slower processors can only execute one instruction per clock cycle, but faster,

- more advanced processors can execute multiple instructions per clock cycle, processing data more efficiently. Each clock cycle is called as T-states.

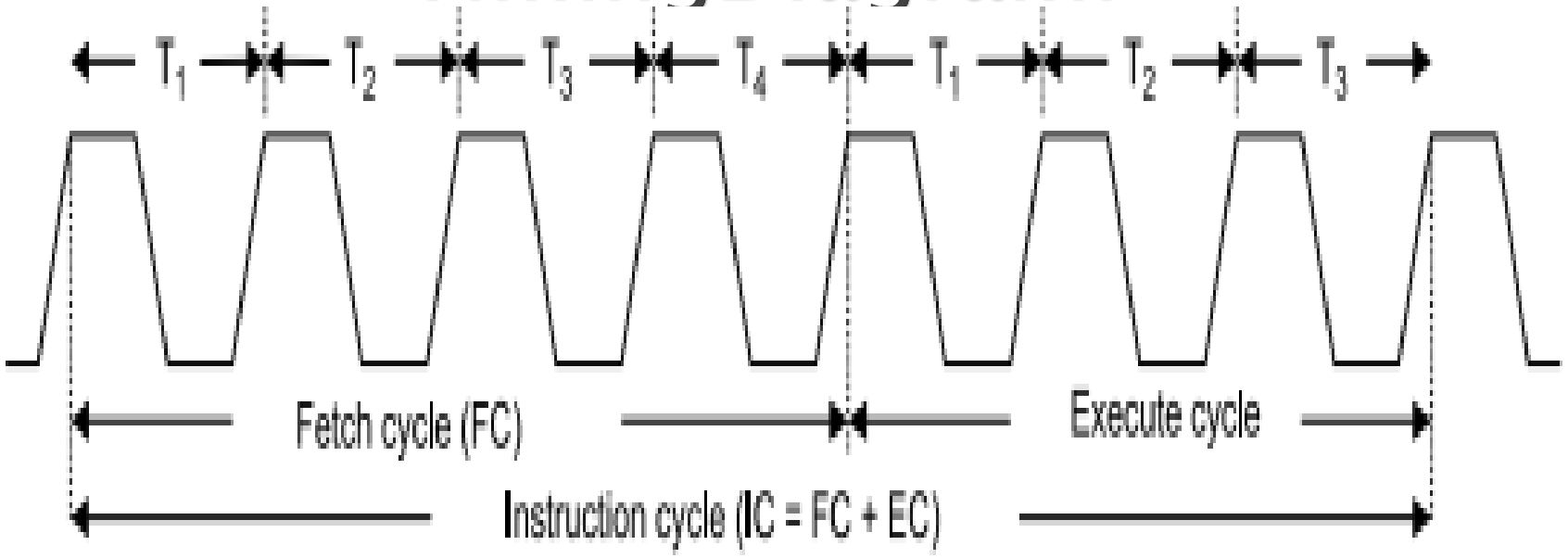
8085 machine cycle & bus timing

2. Instruction cycle

The sequence of operations that the CPU has to carry out while execution is called instruction cycle.

- 1:- Read an Instruction
- 2:- Decode the instruction
- 3:- Find the address of operand
- 4:- retrieve an operand
- 5:- perform desired operation
- 6:- find the address of destination
- 7:- store the result into the destination

TimingDiagram:



- Where, Instruction cycle= Fetch Cycle(FC) (and decode the opcode) + Execute cycle(EC). Performing each cycle needs performing one or more of the machine cycle.

3. Machine cycle:

The steps performed by the computer processor for each machine language instruction. The four common machine cycles are:-

- A. Opcode Fetch – Retrieve an instruction code from the memory.
- B. Memory Read (MR) – Retrieve the operand from the memory.
- C. Memory Write (MW) – Send the result to the memory Store.
- D. Input_Output Read (I/O R) – Read the operand from the Input port.
- E. Input_Output Write (I/O W) – Send the operand from the Input port.

Timing Diagram

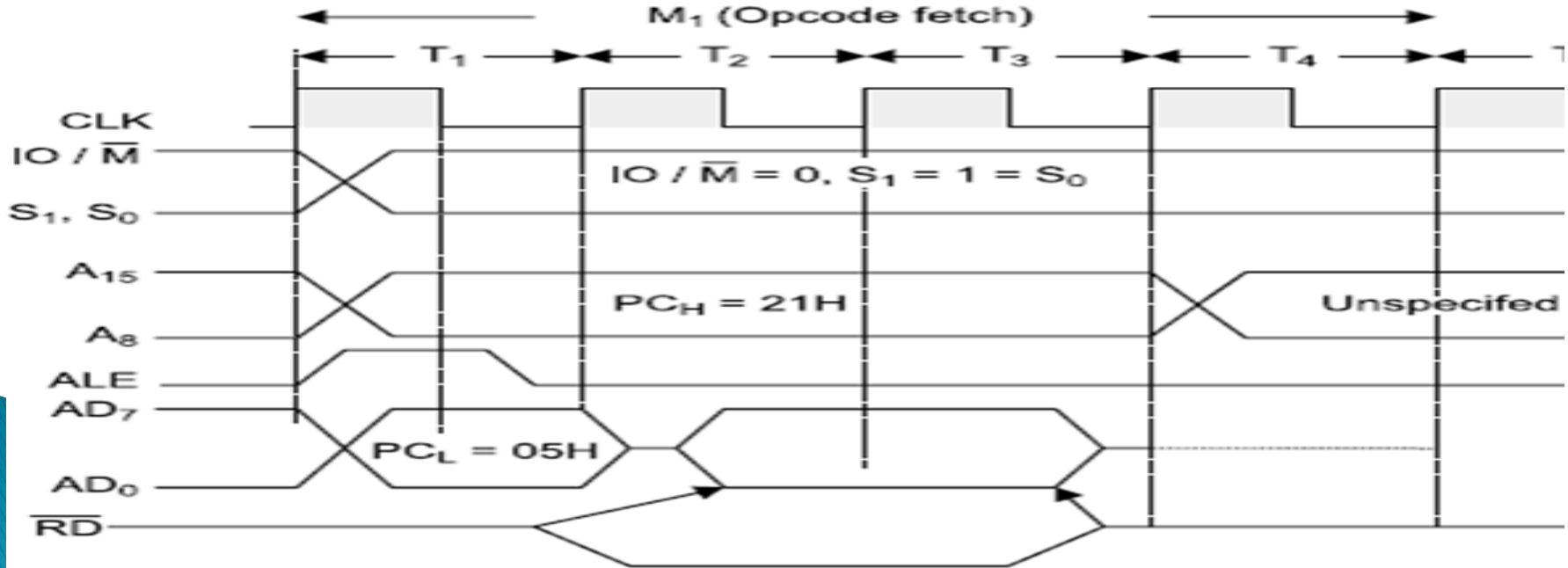
Representation of Various Control signals generated during Execution of an Instruction. Following Buses and Control Signals must be shown in a Timing Diagram:

Higher Order Address Bus. Lower Address/Data bus ALE
RD WR IO/M

Opcode fetch:

The microprocessor requires instructions to perform any particular action. In order to perform these actions microprocessor utilizes Opcode which is a part of an instruction which provides detail (i.e. which operation µp needs to perform) to microprocessor

Figure (2): Opcode fetch timing diagram



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Operation steps:

- 1- During T1 state, $\overline{\quad}$, S0, S1 signals are used to instruct microprocessor to fetch opcode. Thus when $\overline{\quad}$=0, S0=S1= 1, it indicates opcode fetch operation. During this operation 8085 transmits 16-bit address and also uses ALE signal for address latching. A8-A15 contains higher byte of address and lower byte of address A0-A7 is selected from AD0-AD7.
- 2- At T2 & T3 state, microprocessor uses read signal and make data ready from that memory location to read opcode from memory. Address is removed from AD0-AD7 and data D0-D7 appears on AD0-AD7.

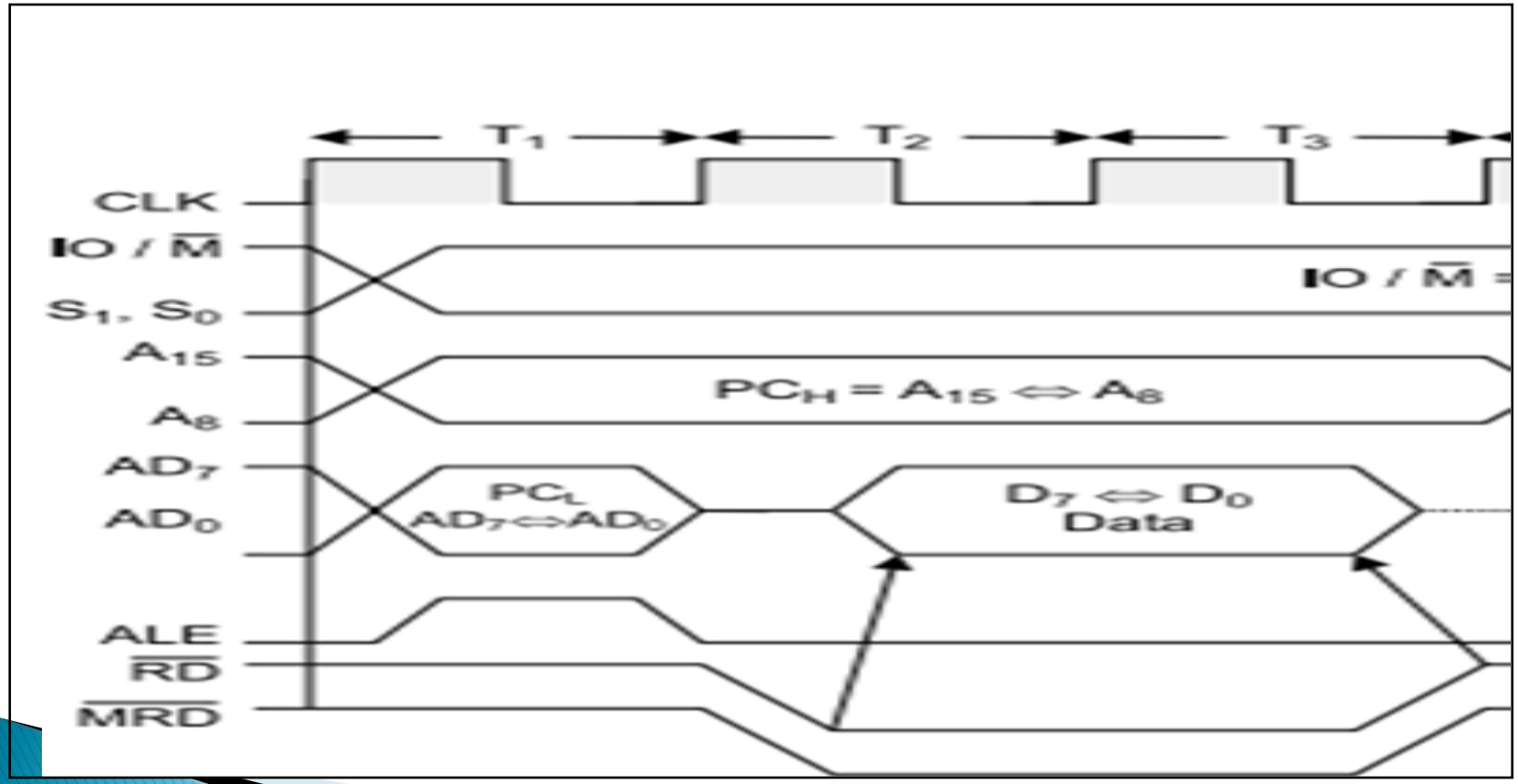
Microprocessor reads opcode and stores it into instruction register to decode it further.

- 3- During T4 microprocessor performs internal operation like decoding opcode and providing necessary actions.

Read and write timing diagram for memory and I/O Operation

- Memory Read:

Figure (3): Memory read timing diagram.



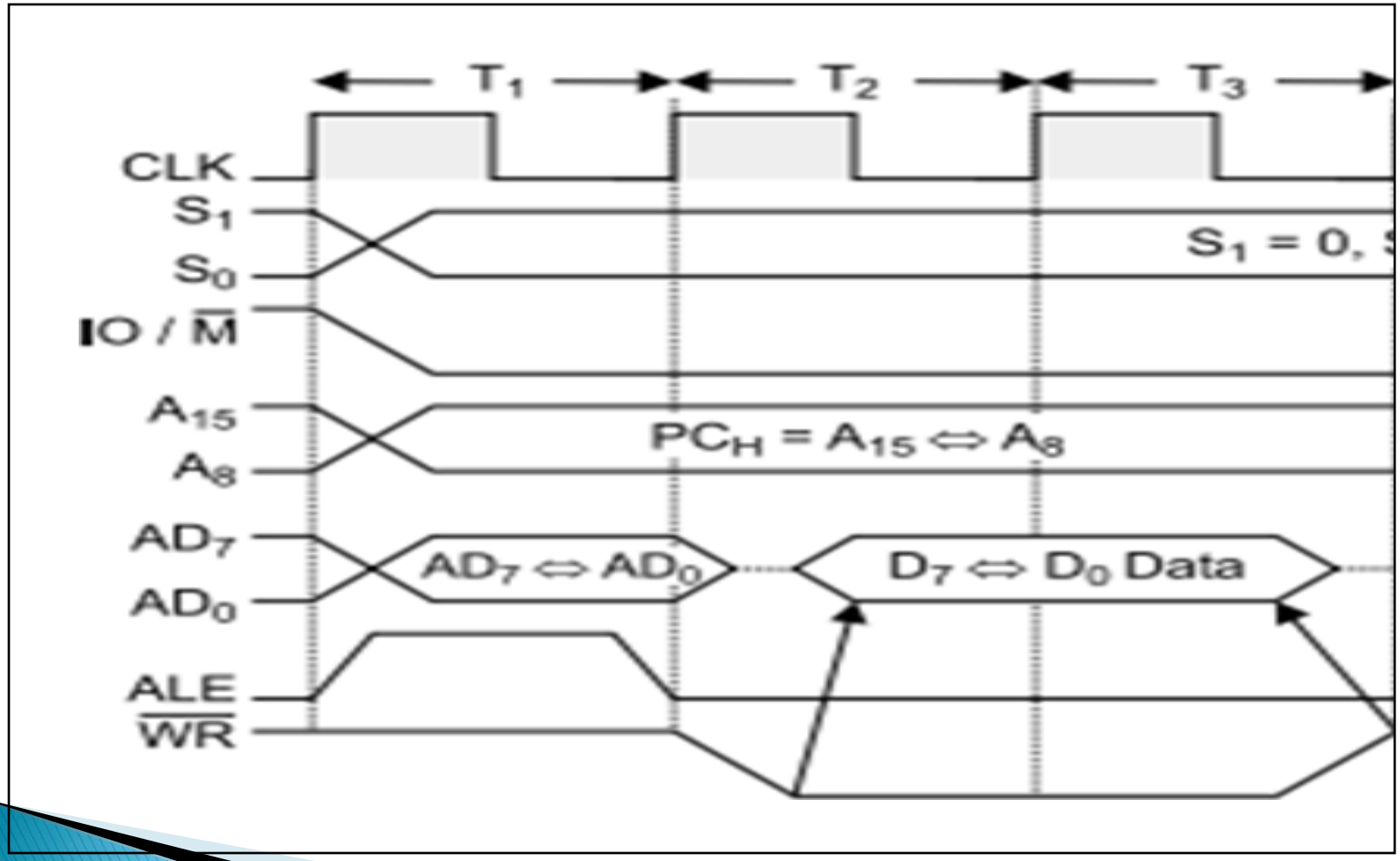
Operation steps:

- 1- It is used to fetch one byte from the memory.
- 2- It requires 3 T-States.
- 3- It can be used to fetch operand or data from the memory.

- 4- During T1, A8-A15 contains higher byte of address. At the same time ALE is high. Therefore Lower byte of address A0-A7 is selected from AD0-AD7.
- 5- Since it is memory ready operation, $\overline{\text{}}$ goes low.
- 6- During T2 & T3, ALE goes low, $\overline{\text{}}$ goes low. Address is removed from AD0-AD7 and data D0-D7 appears on AD0-AD7.

memory write

Figure (4): Memory write timing diagram



Operation:

- 1- It is used to send one byte to memory.
- 2- It requires 3 T-States.
- 3- During T1, ALE is high and contains lower address A0-A7 from AD0-AD7.
- 4- A8-A15 contains higher byte of address.
- 5-As it is memory operation, $\overline{\text{}}$ goes low.
- 6-During T2 & T3, ALE goes low, $\overline{\text{}}$ goes low and Address is removed from AD0-AD7 and then data appears on AD0-AD7.