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College of Engineering and Technologies
Medical Instrumentation Technique Engineering Department
Class: 2nd
Subject: Electronic Circuits
Lecturer: Dr. Rami Qays Malik
Lecture: 4- Diode Applications (half & full wave rectification)

Diode Applications

HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. The process of removing one-half the input signal to establish a dc level is called **half wave rectification** .The simplest of networks to examine with a time-varying signal appears in Fig. 2.44 . For the moment we will use the ideal model (note the absence of the Si, Ge, or GaAs label) to ensure that the approach is not clouded by additional mathematical complexity.

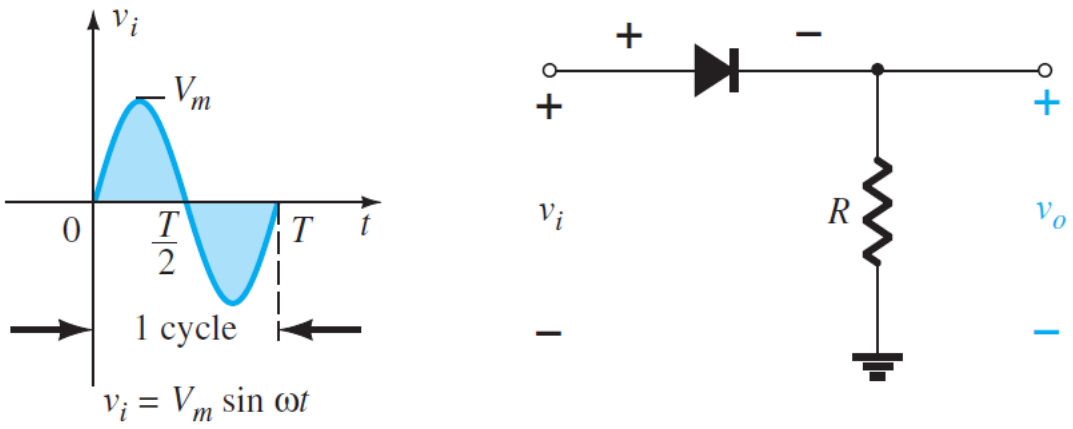

FIG. 2.44
Half-wave rectifier.

During the interval t = 0ST>2 in Fig. 2.44 the polarity of the applied voltage v i is such as to establish pressure in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.45 , where it is fairly

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obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode. For the period T>2ST, the polarity of the input v i is as shown in Fig. 2.46 , and the resulting polarity across the ideal diode produces an off state with an open-circuit equivalent. The result is the absence of a path for charge to flow, and vo = iR = (0)R = 0 V for the period T>2ST. The input vi and the output v o are sketched together in Fig. 2.47 for comparison purposes. The output signal v o now has a net positive area above the axis over

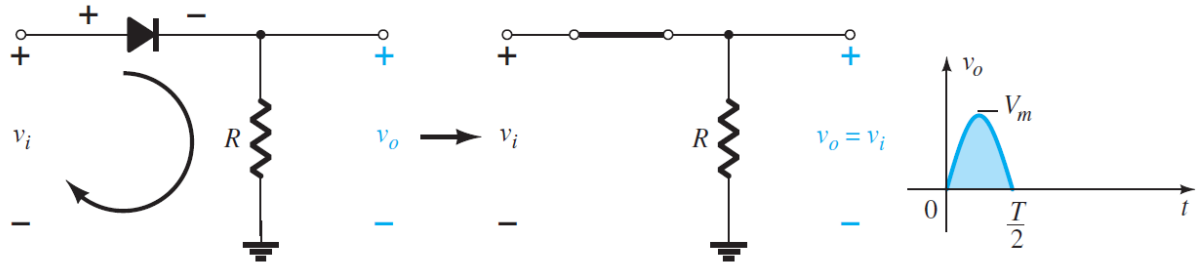

FIG. 2.45
Conduction region (0 → T/2).

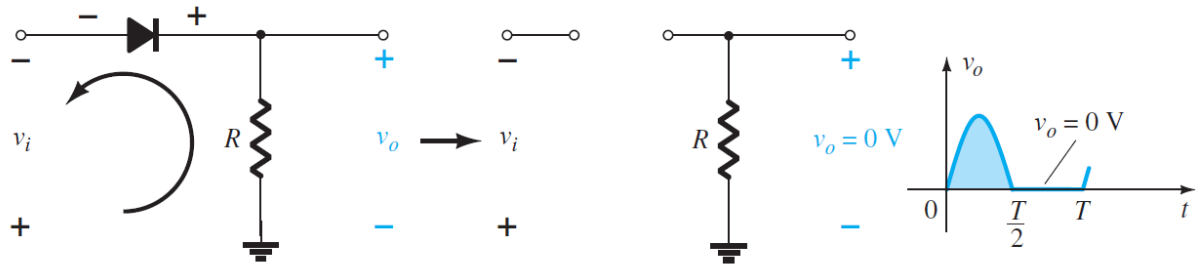

FIG. 2.46
Nonconduction region (T/2 → T).

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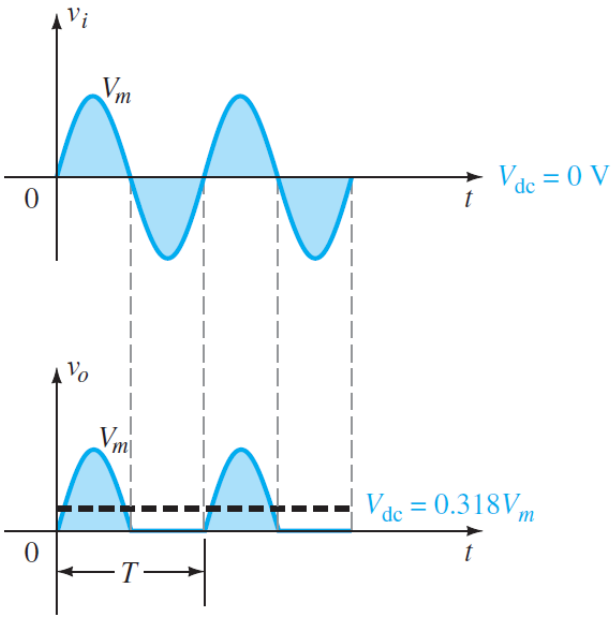

FIG. 2.47
Half-wave rectified signal.

a full period and an average value determined by

$$V_{dc} = 0.318\,V_m \quad \text{half-wave}$$

The effect of using a silicon diode with V K 0.7 V is demonstrated in Fig. 2.48 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn For levels of v i less than 0.7 V, the diode is still in an open circuit state and v o 0 V, as shown in the same figure. When conducting, the difference between v o and v i is a fixed

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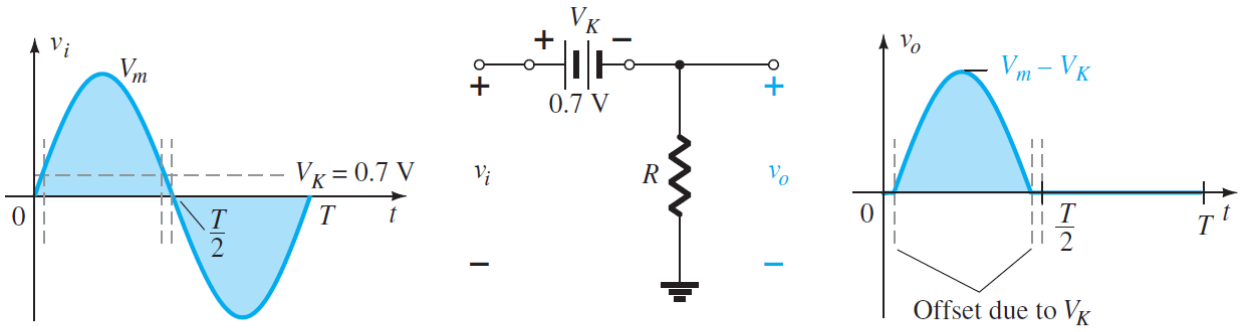

FIG. 2.48
Effect of V_K on half-wave rectified signal.

level of V K = 0.7 V and vo = vi - VK, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where Vm << VK, the following equation can be applied to determine the average value with a relatively high level of accuracy

$$V_{dc} \cong 0.318(V_m - V_K)$$

EXAMPLE 1

a. Sketch the output v o and determine the dc level of the output for the network of Fig. 2.49 .

b. Repeat part (a) if the ideal diode is replaced by a silicon diode.

c. Repeat parts (a) and (b) if V m is increased to 200 V, and compare solutions.

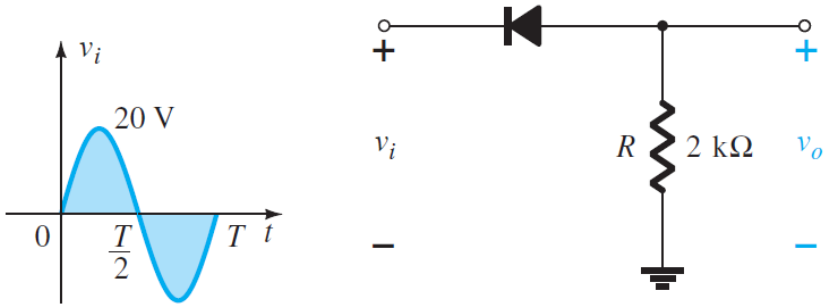

FIG. 2.49

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Solution:

a. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50 , and v o will appear as shown in the same figure. For the full period, the dc level is

Vdc = - 0.318 Vm = -0.318(20 V) = - 6.36 V

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.49.

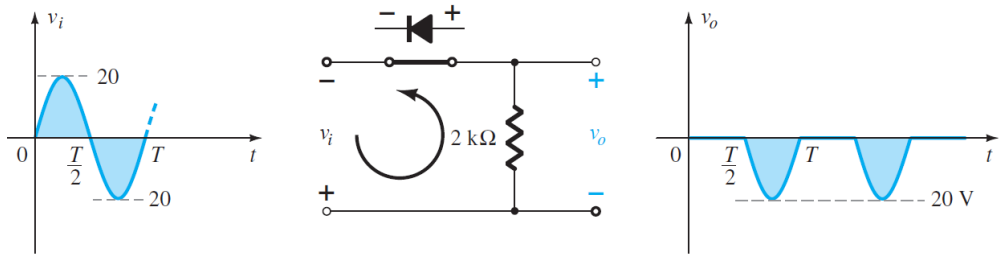

FIG. 2.50

b. For a silicon diode, the output has the appearance of Fig. 2.51, and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V, or about 3.5%.

c. Eq. (2.7): $V_{dc} = -0.318\,V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_K) = -0.318(200\text{ V} - 0.7\text{ V})$

$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

FULL-WAVE RECTIFICATION

1. Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification . The most familiar network for

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performing such a function appears in Fig. 2.53 with its four diodes in a bridge configuration

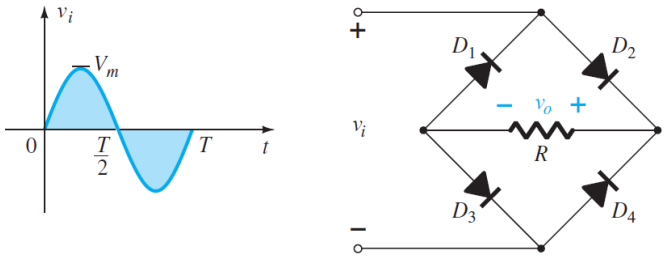


FIG. 2.53
Full-wave bridge rectifier.

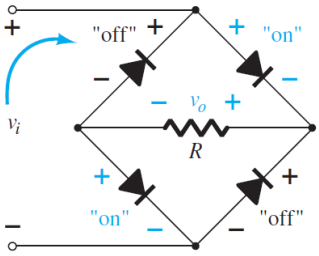


FIG. 2.54
Network of Fig. 2.53 for the period $0 \rightarrow T/2$ of the input voltage v_i.

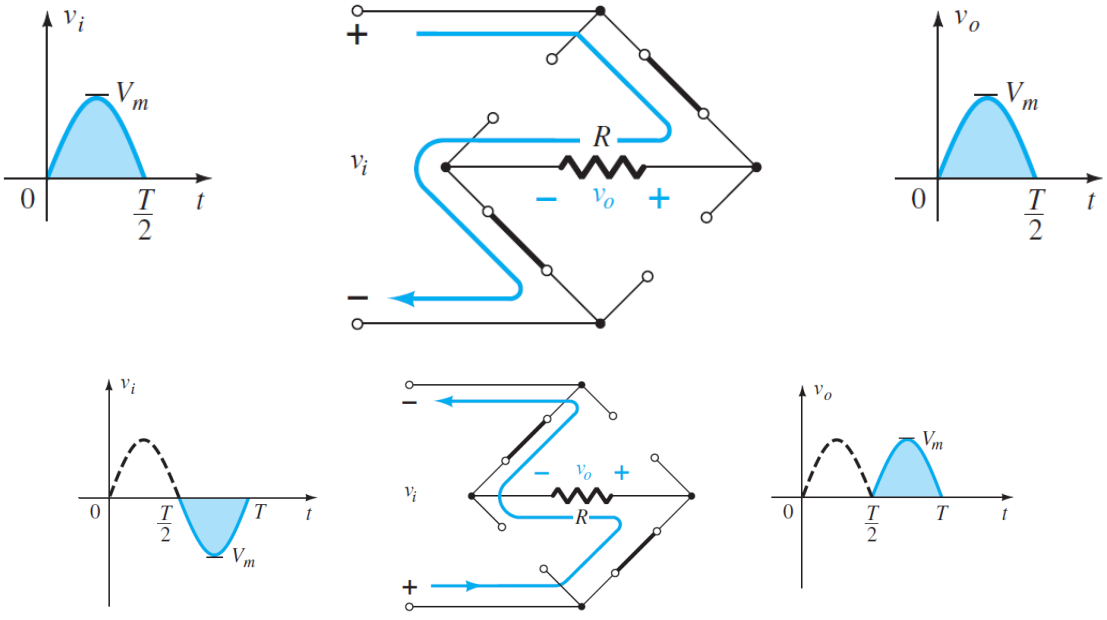
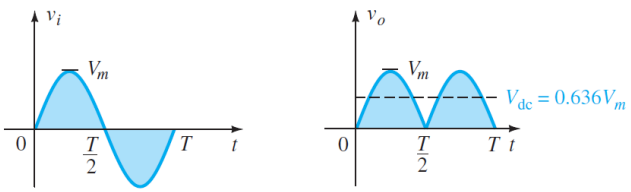


FIG. 2.56
Conduction path for the negative region of v_i.



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Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

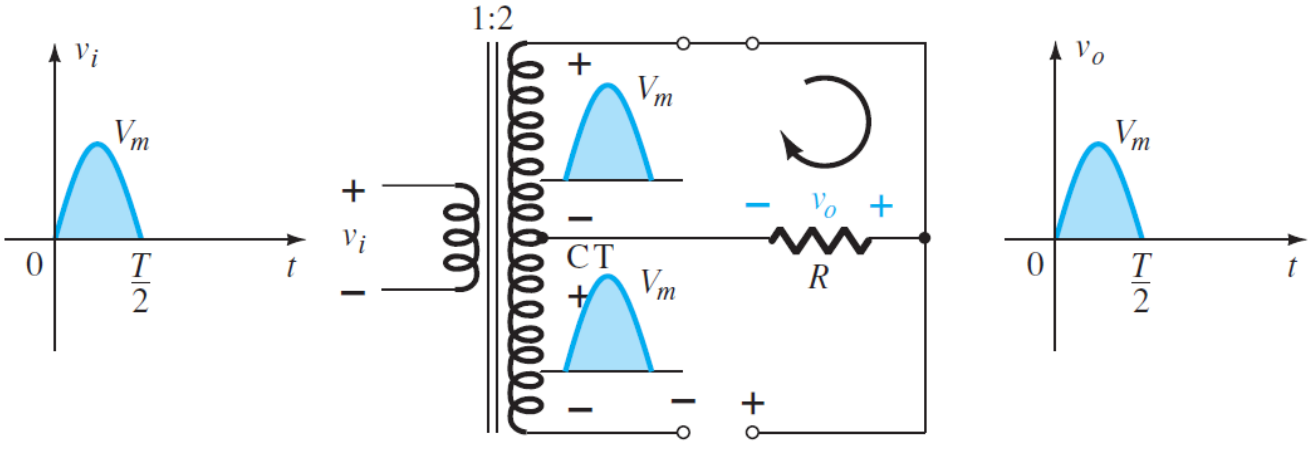
$$V_{dc} = 0.636\,V_m$$ full-wave

If silicon rather than ideal diodes are employed, the application of Kirchhoff's voltage law around the conduction path results in

$$V_{dc} \cong 0.636(V_m - 2V_K)$$

2. Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v i applied to the primary of the transformer, with a positive pulse across each section of the secondary coil. D 1 assumes the short-circuit equivalent and D 2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions.



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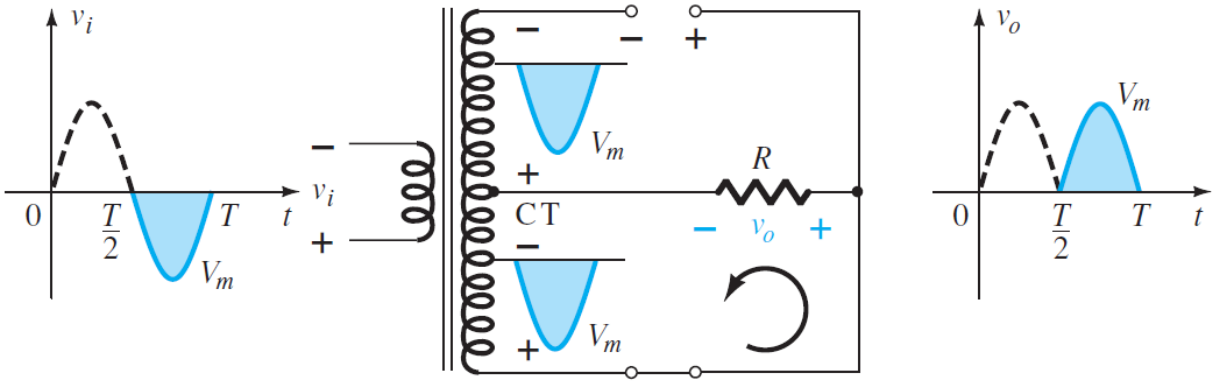
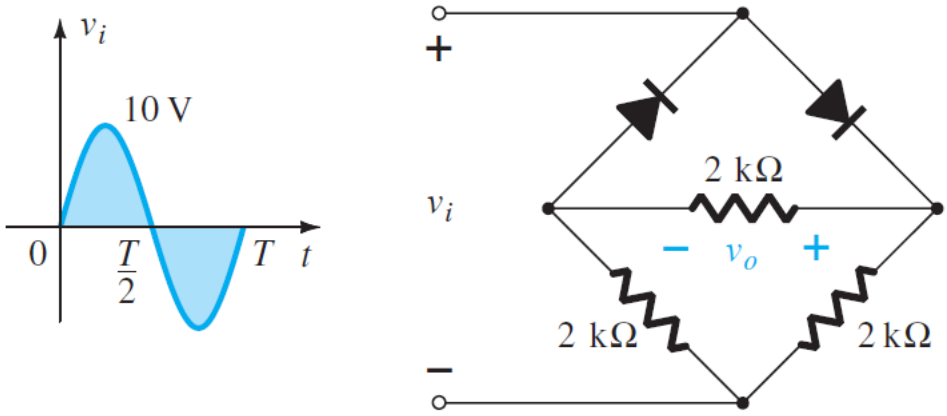


EXAMPLE

Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level.



Solution: The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where $v_o = \frac{1}{2}v_i$ or $V_{o_{max}} = \frac{1}{2}V_{i_{max}} = \frac{1}{2}(10\text{ V}) = 5\text{ V}$, as shown in Fig. 2.66. For the negative part of the input, the roles of the diodes are interchanged and v_o appears as shown in Fig. 2.67.

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{dc} = 0.636(5\text{ V}) = \mathbf{3.18\text{ V}}$$

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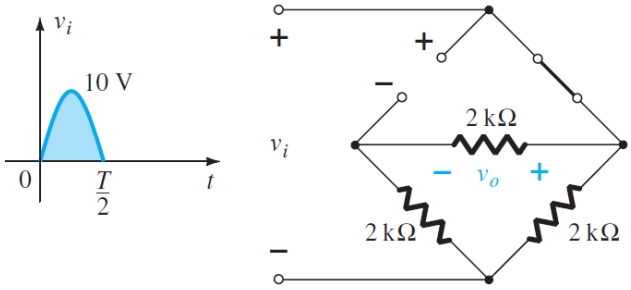

FIG. 2.65
Network of Fig. 2.64 for the positive region of v_i.

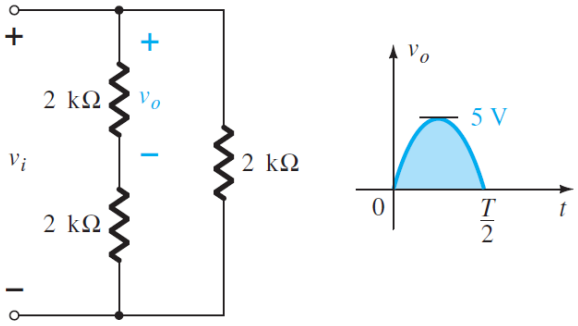

FIG. 2.66
Redrawn network of Fig. 2.65.

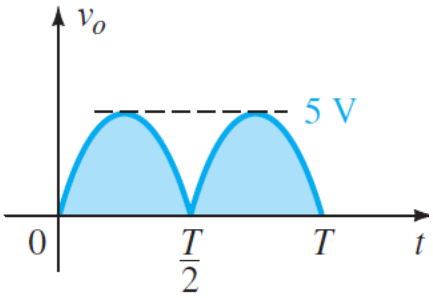

FIG. 2.67
Resulting output for Example .

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