Ministry of Higher Education and Scientific Research

Al-Mustaqbal University College

Computer Engineering Techniques Department

Subject: Digital Communications

Class: 3rd

Lecture Seven

"Pulse Modulation Techniques 2"

By

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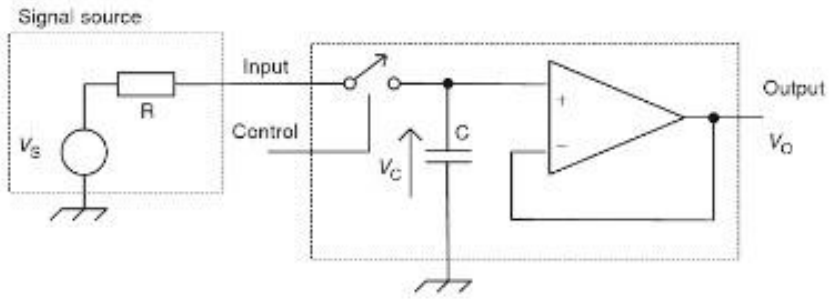
❖ ***Sample and Hold Circuit***

Figure below shows the sample and hold circuit that produces a PAM signal



The switch closes only when that particular channel is to be sampled. If the source impedance **r** is small, the capacitor voltage changes to the input voltage within the time τ that switch is closed.

The load impedance **R** is arranged to be high so that the capacitor retains the voltage level until the switch is closed again. Therefore the sample and hold circuit accepts only those values of the input which occur at the sampling times and then holds them until the next sampling time.

Example:

Channel 1 of two channels PAM system handles 8KHz signal. Channel 2 handles 10 KHz signals. The two channels are sampled at equal intervals of time using very narrow pulses at the lowest frequency that is theoretical adequate. The sampled signals are time multiplexed and passed through a LPF before transmission.

(1)What is the minimum clock frequency of the PAM system?

(2)What is the minimum cut off frequency of LPF used before transmission that will preserve the amplitude information on the output pulses?

(3) What would be the minimum bandwidth if these channels were frequency multiplexed, using AM technique and SSB technique?

Solution

(1)

$$f_{s1} = 2 * f_{m1}$$

$$f_{s1} = 2 * 8 = 16KHz$$

$$f_{s2} = 2 * f_{m2}$$

$$f_{s2} = 2 * 10 = 20KHz$$

In order to sample channel 2 adequately

$$f_s = f_{s2} = 20KHz$$

$\therefore$ The minimum clock rate $= n * f_s$

$$= 2 * 20 = 40KHz$$

(2)

$$T_s = \frac{1}{f_s} = \frac{1}{20KHz} = 50\mu\text{sec}$$

$\square\ n = 2$

$$T_x = \frac{T_s}{n} = \frac{50}{2} = 25\mu\text{sec}$$

$\square\ B_x \geq \frac{1}{2T_x}$

$\therefore B_x = 20KHz$

(4) For AM

$$\min.BW. = 2(f_{m1} + f_{m2}) = 2(8+10) = 36KHz$$

For SSB

$$\min.BW. = f_{m1} + f_{m2} = 8+10 = 18KHz$$

H.W

Two low pass signals, each band limited 4KHz, are to be time multiplexed into a single channel using PAM. Each signal is impulse sampled at a rate 10KHz. The time multiplexed signal waveform is filtered by an ideal LPF before transmission.

(a) What is minimum clock frequency of the system?

(b) What is the minimum cut off frequency of the LPF?

(c) In the receiver side, determine the minimum and maximum acceptable bandwidth of the LPF used in retrieving the analog signal?

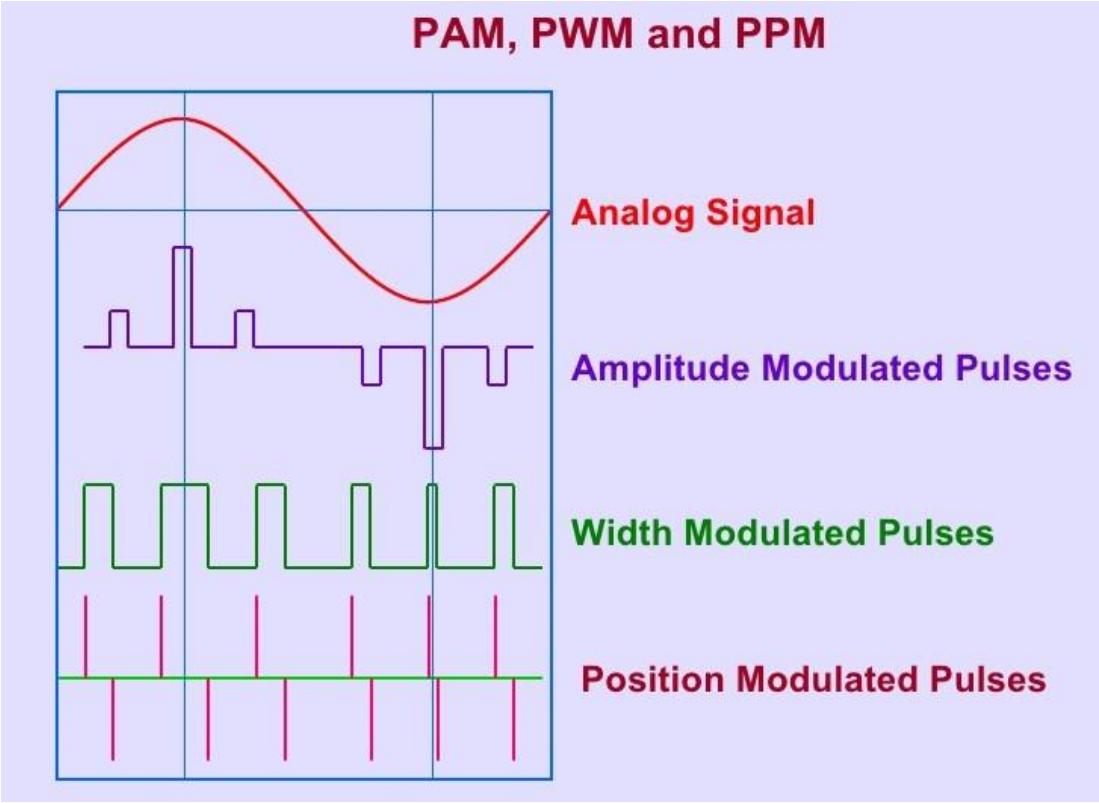
Ans. (a) 20KHz (b) 10KHz (c) 4KHz, 6KHz.

(2) Other Types of Analog Pulse Modulation (PWM&PPM)

One type of pulse timing modulation uses constant amplitude pulses whose width is proportional to the value of message signal at the sampling instants. This type is designated as ***pulse width modulation (PWM) or pulse duration modulation (PDM)*** is also called.

Another possibility is to keep both the amplitude and the width of the pulses constant but vary the pulse position in proportion to the value of message signal at sampling instant. This is designated as ***pulse position modulation (PPM)***.

PAM, PWM and PPM waveforms for a given message signal are shown below: -

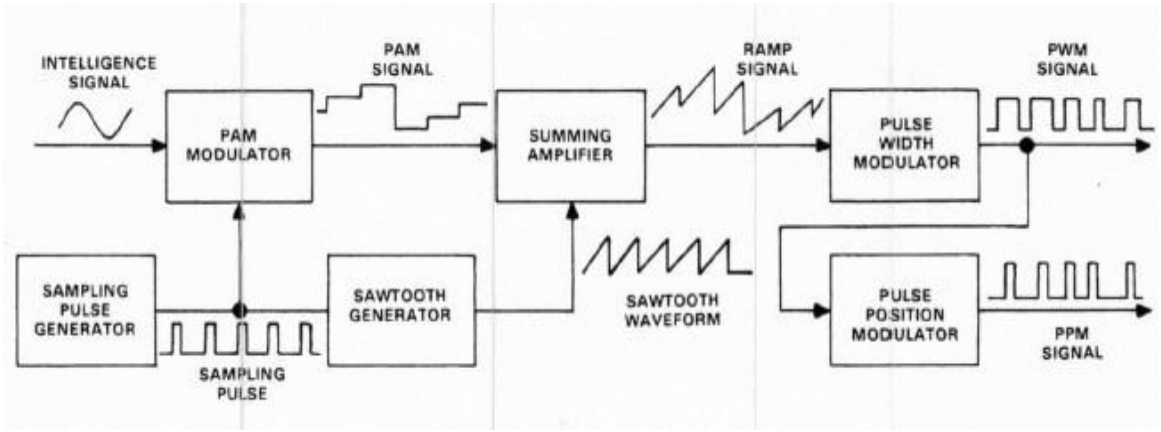


In PWM, the signal f(t) is sampled periodically at a rate fast enough to satisfy the requirements of the sampling theorem. At each sampling instant a pulse is generated with fixed amplitude and a width that is proportional to the sample value of f(t). A minimum pulse width is assigned to the minimum value of f(t).

In PPM, these are sent as constant width, constant amplitude pulses. The minimum pulse delay is used to designate the minimum value of f(t) and the change in delay is proportional to the modulating signal. The constant of proportionality is the modulation constant.

Generation of PWM & PPM

Generation of PWM and PPM commonly employs various combinations of a sample and holed circuit, a precision ramp voltage generator and a comparator. The block diagram of a typical circuit for generation PWM and PPM is shown in figure below: -



The ramp generator produces a precision ramp voltage which has peak to peak amplitude slightly larger than the maximum amplitude range of the input signals. This ramp voltage is the basis for the amplitude to timing conversion and therefore must be accurately known.

The comparator is a high gain amplifier intended for two stated operation. If input signal is higher than a preset reference level, the output is held in one state (i.e. a given voltage level). Whenever the input signal level is less than the reference level, the output is held in the other state. Which output state is present, then, depends upon whether the input is above and below the threshold (reference level) of the comparator.

The voltage reference level of the comparator is adjust so that there is always an intersection with the sum of the sample and hold circuit and ramp voltage. In this system, the first crossing of the reference level indicates the clock timing and the second crossing generates the variable trailing edge.

A convenient way to generate PPM is to use PWM waveform generated above and then trigger a constant width pulse generation those edge of the PWM waveform with a negative slope.