Analog electronics

Sixth lecture

Junction Field Effect Transistor (JFET).

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Outline

6.1. Field Effect Transistor

A Field Effect Transistor (FET) is a three terminal active device that uses an electric field to control the current flow and it has a high input resistance which is useful in many circuits. Its operation is based on a controlled input voltage.

FETs are also known as unipolar transistors since they involve single-carrier-type operation. That is, FETs use either electrons (n-channel) or holes (p-channel) as charge carriers in their operation, but not both. A FET is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless signals).

Most commonly two types of FETs are available.

1- Junction Field Effect Transistor (JFET).

2- Metal Oxide Semiconductor FET (MOSFET).

6.2. Junction Field Effect Transistor (JFET)

JFET is one of the simplest types of field-effect transistor. Contrary to the Bipolar Junction Transistor, JFETs are voltage-controlled devices. In JFET, the current flow is due to the majority of charge carriers.

The functioning of Junction Field Effect Transistor depends upon the flow of majority carriers (electrons or holes) only. Basically, JFETs consist of an N-type or P-type silicon bar containing PN junctions at the sides. There are two types of JFETs commonly used in the field semiconductor devices: N-Channel JFET and P-Channel JFET. FET has three terminals which are:

Source: is the terminal through which the majority charge carriers are entered in the FET.

Drain: is the terminal through which the majority charge carriers exit from the FET.

Gate: is formed by diffusion of an N-type semiconductor with a P-type semiconductor. This creates a heavily doped PN junction region that controls the flow of the carrier from source to drain.

Body: This is the substrate on which the FET is built.

Channel: This is the region in which the majority carriers pass from the source terminal to the drain terminal.

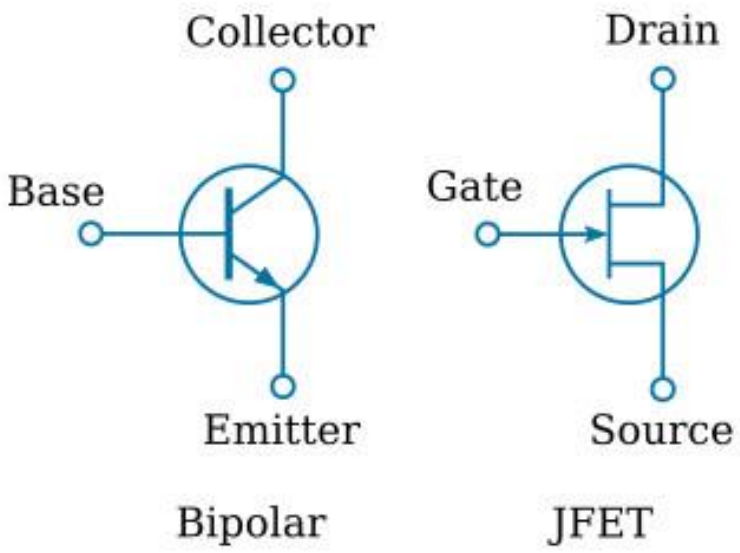

Figure 1: Comparison of JFET (N-channel) and bipolar transistor (NPN) symbols.

6.2.1. N-Channel JFET

It has major portion made of n-type semiconductor into which embedded are the two small p-type regions. Thus it has an p-type gate terminal and n-type source and drain, causing the channel to be of n-type where the electrons will be the majority charge carriers.

Following figure shows the crystal structure and schematic symbol of an N-channel JFET. Then the gate is formed on top of the N-channel with P-type material. At the end of the channel and the gate, lead wires are attached and the substrate has no connection.

When a DC voltage source is connected to the source and the drain leads of a JFET, maximum current will flow through the channel. The same amount of current will flow from the source and the drain terminals. The amount of channel current flow will be determined by the value of V_{DD} and the internal resistance of the channel.

A typical value of source-drain resistance of a JFET is quite a few hundred ohms. It is clear that even when the gate is open full current conduction will take place in the channel. Essentially, the amount of bias voltage applied at I_D, controls the flow of current carriers passing through the channel of a JFET. With a small change in gate voltage, JFET can be controlled anywhere between full conduction and cutoff state.

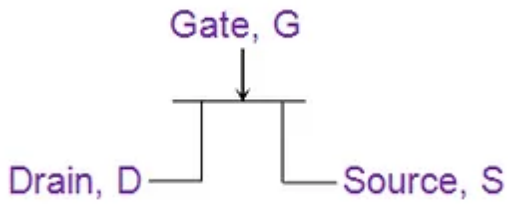

Figure (2) N-channel JFET Circuit Symbol

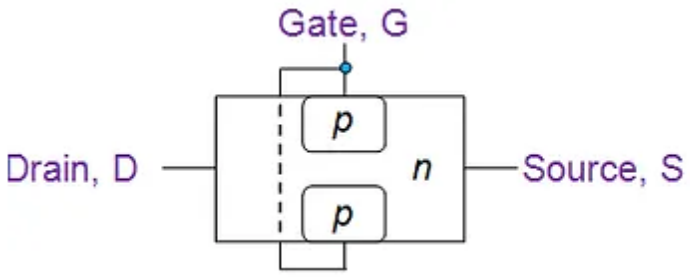

Figure (3) N-channel JFET Layered Structure

Working of N-channel JFET

In n-channel JFET, the majority charge carriers will be the electrons as the channel formed in-between the source and the drain is of N-type. Further, the working of these devices depends upon the voltages applied at its terminals

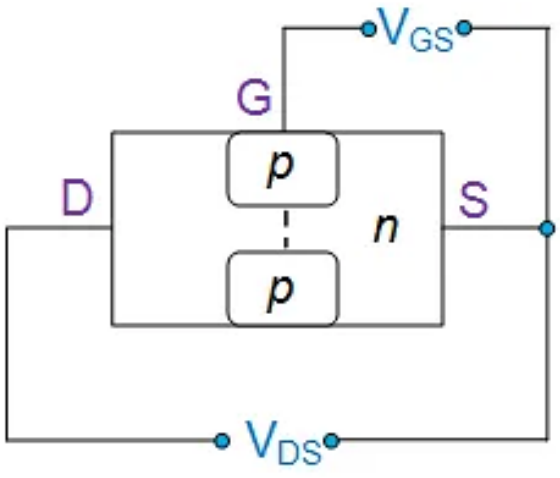

Figure (4) N-channel JFET in Biased state.

6.2.2. P-Channel JFET

It has major portion made of p-type into which embedded are the two small n-type regions. Thus it has an n-type gate terminal and p-type source and drain, causing the channel to be of p-type where the holes will be the majority charge carriers.

The gate is formed on top of the P-channel with N-type material. At the end of the channel and the gate, lead wires are attached. Rest of the construction details are similar to that of N-channel JFET

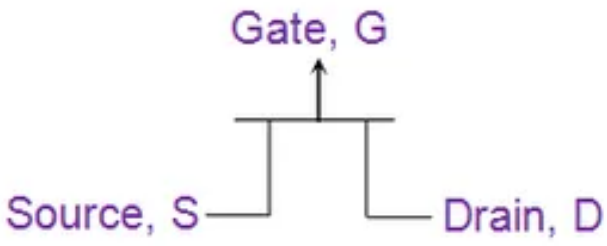

Figure (5) P-channel JFET Circuit Symbol.

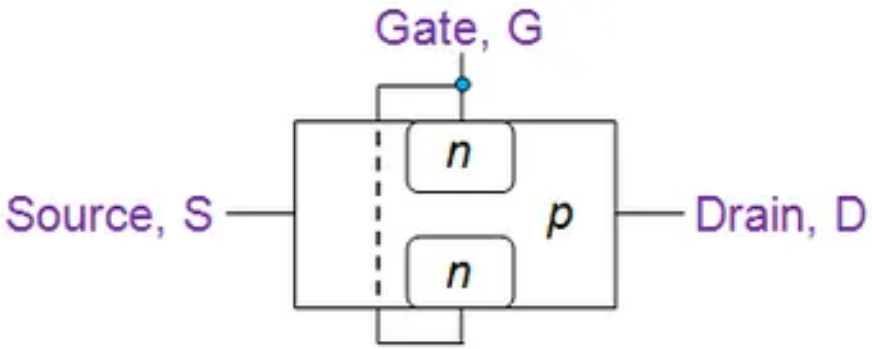

Figure (6) P-channel JFET Layered Structure.

6.3. Output characteristic curves of JFET

The characteristics curve of a JFET transistor is the the curve which shows the graph of the drain current, I_D verses the drain - source voltage, V_{DS}, for different values of gate - source voltage V_{GS}.

The V-I characteristics of N-channel JFET are shown below. In this N-channel JFET structure the gate voltage (V_{GS}) controls the current flow between the source drain. The JFET is a voltage controlled device so no current flows through the gate, then the source current (I_S) is equal to the drain current (I_D) i.e. $I_D = I_S$. In this V-I characteristic the voltage V_{GS} represents the voltage applied between the gate and the source and the voltage V_{DS} represents the voltage applied between the drain and source.

The Regions that make up a transconductance curve are the following:

Cutoff Region- This is the region where the JFET transistor is off, meaning no drain current I_D flows from drain to source.

Ohmic Region- This is the region where the JFET transistor begins to show some resistance to the drain current I_D that is beginning to flow from drain to source. This is the only region in the curve where the response is linear.

Saturation Region- This is the region where the JFET transistor is fully operation and maximum current, for the voltageV_{GS}, that is supplied is flowing. During this region, the JFET is On and active.

Breakdown Region- This is the region where the voltage, V_{DD} that is supplied to the drain of the transistor exceeds the necessary maximum. At this point, the JFET loses its ability to resist current because too much voltage is applied across its drain-source terminals. The transistor breaks down and current flows from drain to source.

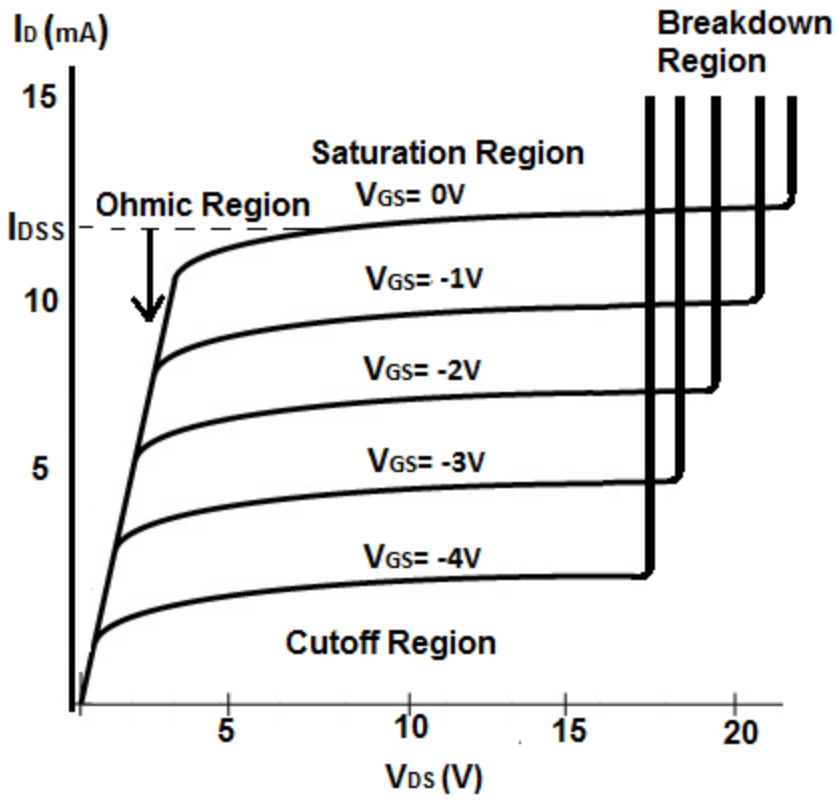

Figure 7: I-V Characteristics curve of JFET.

6.4. JFET small signal parameters

Table. 1 displays the details of the JFET parameters:

Parameter	Equation	Unit	Range
AC drain resistance, rd (Dynamic resistance)	$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}	Ω	Very high (10 kΩ-1 MΩ)
Transconductance,gm (Forward transfer conductance)	$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS}	S	Very low (150-250)S
Amplification factor,	$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ at constant I_D	No unit	High (100)

The parameters follow the relationship given by the following equation:

$$\mu = r_d \, g_m$$

JFETs are an ideal replacement for BJTs, especially at low frequencies. At low frequency, the input resistance is so high that it provides a better amplification process. The noise level is also comparatively less for low-frequency operation. As we know, I_D can be controlled by varying V_{GS} and V_{DS}, the Taylor series expansion of I_D can be written as equation :

$$\Delta i_D = \frac{\delta i_D}{\delta v_{GS}} \Big|_{V_{DS}} \Delta v_{GS} + \frac{\delta i_D}{\delta v_{DS}} \Big|_{V_{GS}} \Delta v_{DS}$$

Replacing the ratios by JFET parameters from Table above and quantities by small-signal notations i_D, v_{GS} and v_{DS} in equation above, equation is obtained as:

$$i_d = g_m v_{gs} + \frac{1}{r_d} \, v_{ds}$$

The small-signal model of JFETs satisfies equation above.

The behavior of the JFET analyzed using the small-signal model leads to the design of FET circuits with better performance. Performing small-signal analysis of JFET before fabricating the amplifier circuits. The selection of V_{DS} and V_{GS} after understanding the I_D function and its correlation with JFET parameters can help you to achieve a stable amplifier operation.

6.5. **References**

Electronics principles (fourth edition) by Malvino.