LECTURE 8

Clamping Circuits

Analog Electronics

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By

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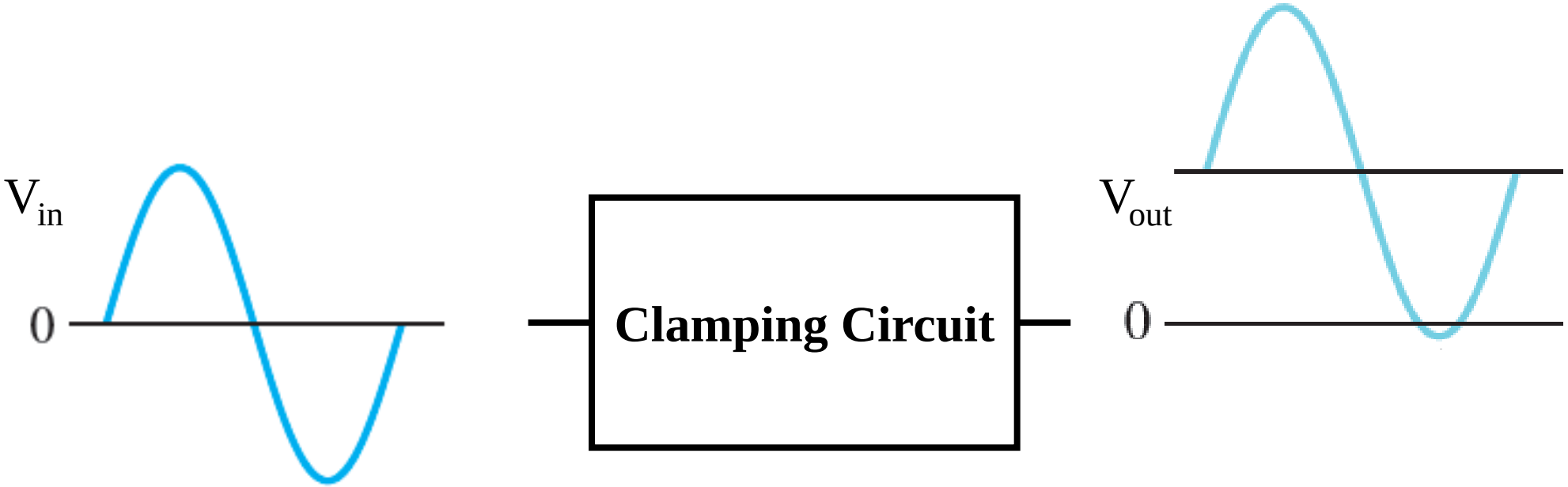
Outline and Aim

After completing this lecture, you should be able to:

- Describe the operation of a passive clamping circuit
- Describe the operation of an active clamping circuit
- Describe the RC time constant
- Describe the operation of an active positive clamper with nonzero reference

Clamping Circuits

The Basic Diode Clamper is used to add a DC level to a signal voltage.
For Example:



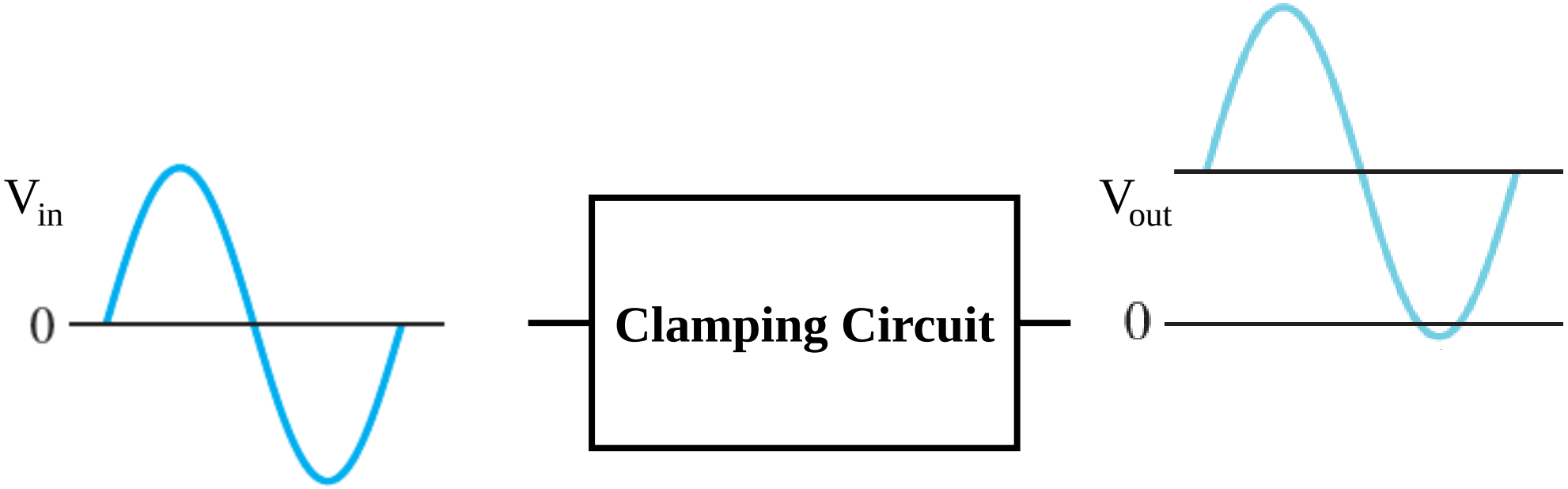
AC signal

AC + DC signal

Clamping Circuits

There are two kinds of the clamping circuit:

1. Passive diode clamping circuit: with a capacitor and a diode
2. Active Clamping Circuit: with a capacitor, an op-amp, and a diode



AC signal

AC + DC signal

Passive diode clamping circuit

To illustrate the basic principle of clamper operation, Fig. 1 shows a simple passive diode clamping circuit that adds a positive DC level to the input signal.
To understand the operation of this circuit, start with the first negative half-cycle of the input voltage.

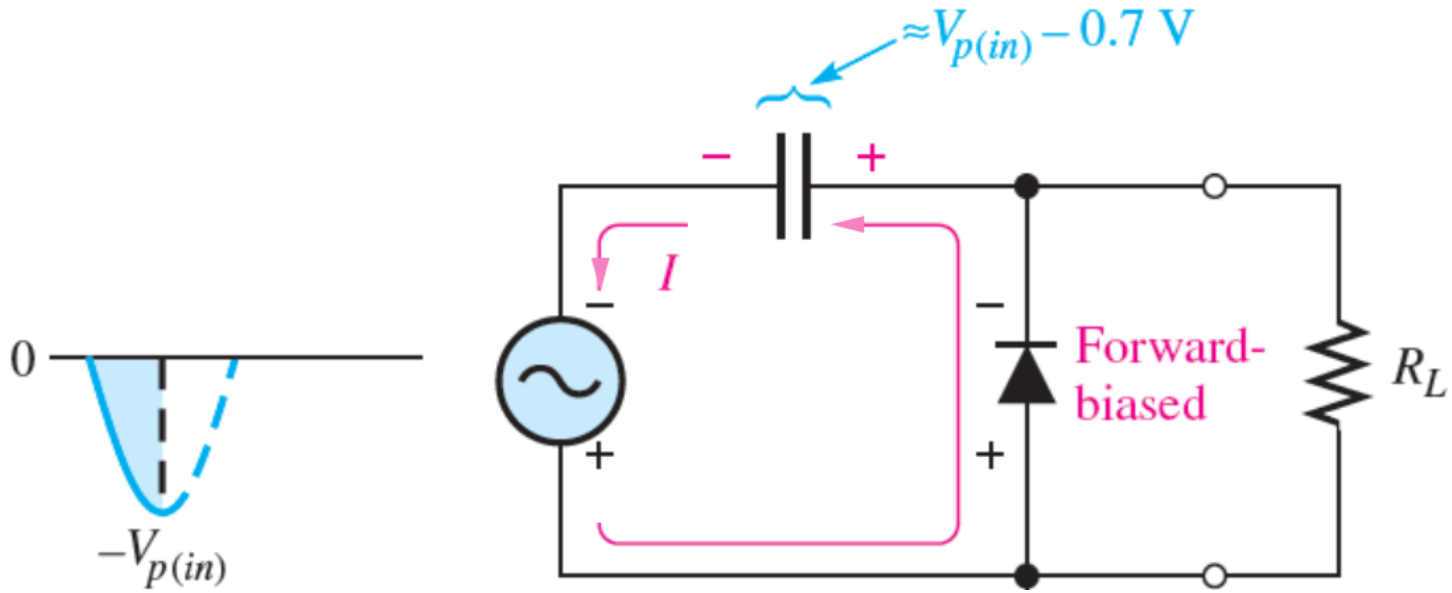


Fig. 1: Positive clamping operation with a passive clamper.

Passive diode clamping circuit

When the input initially goes **negative**, the diode is **forward-biased**, allowing the capacitor to charge to near the peak of the input.

Just past the negative peak, the diode becomes **reverse-biased** because the cathode is held to ($V_{p(in)} - 0.7$) by the charge on the capacitor.

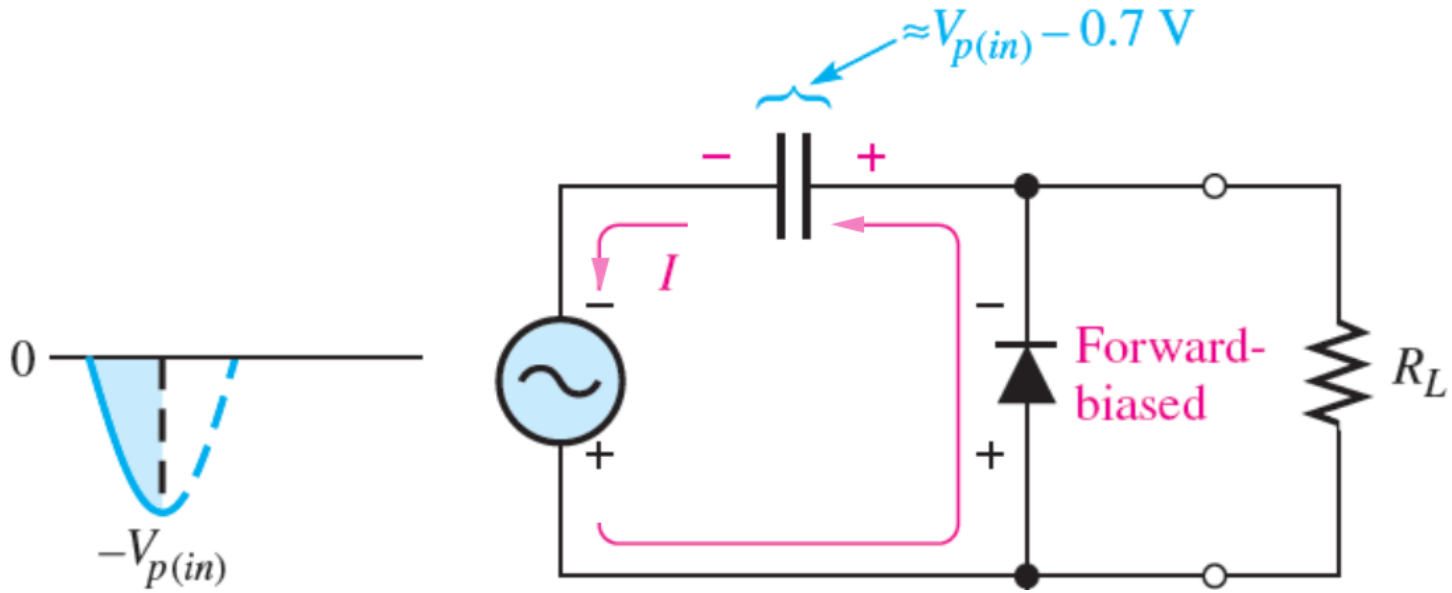


Fig. 1: Positive clamping operation with a passive clamper.

Passive diode clamping circuit

The capacitor can discharge only through R_L. Thus, from the peak of one negative half cycle to the next, the capacitor discharges very little.

The amount that is discharged depends on the value of R_L and the period of the input signal.

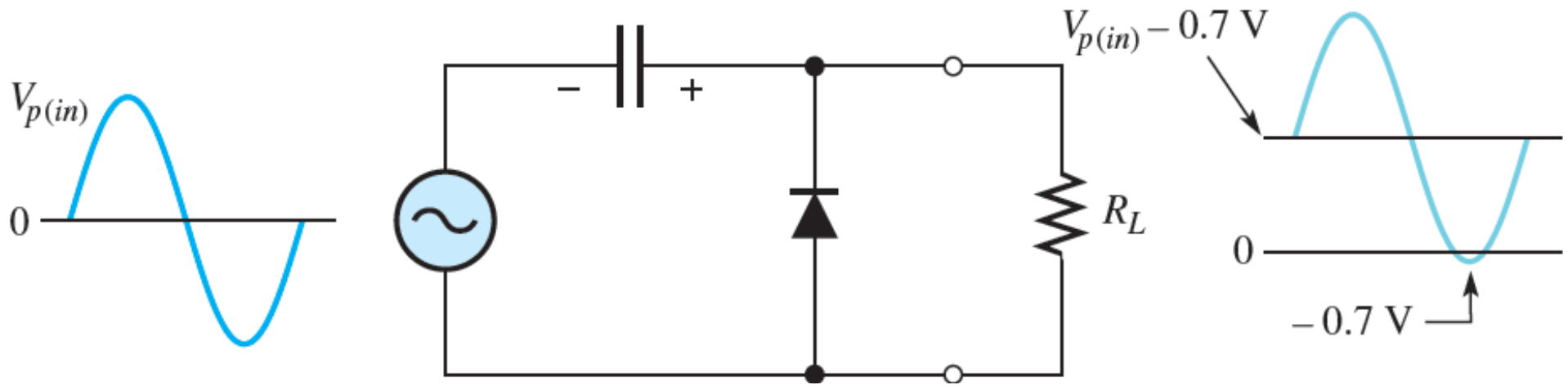


Fig. 2: Positive clamping operation with a passive clamper.

Passive diode clamping circuit

For good clamping action, the RC time constant should be at least **ten times** the period of the input.

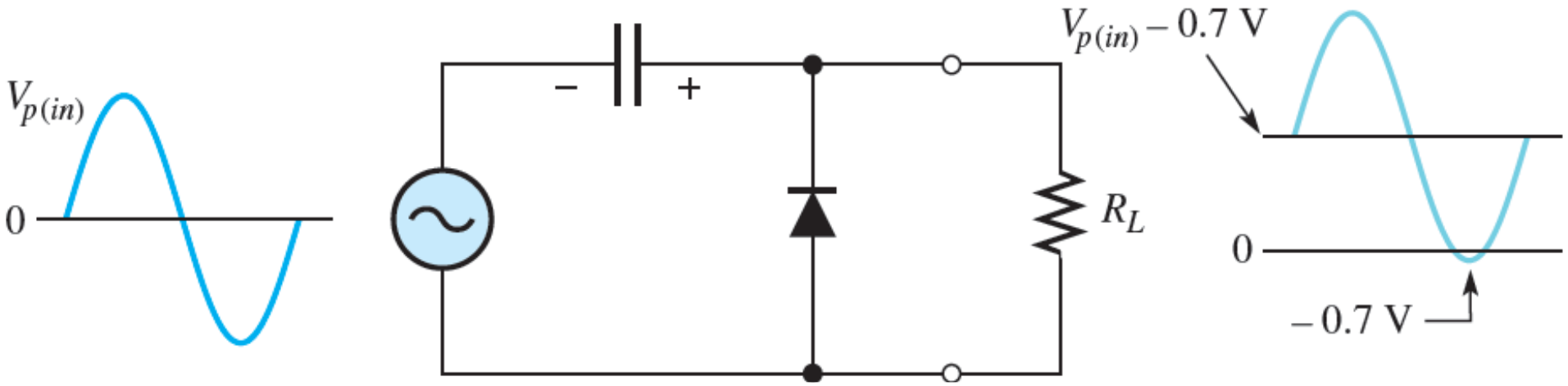
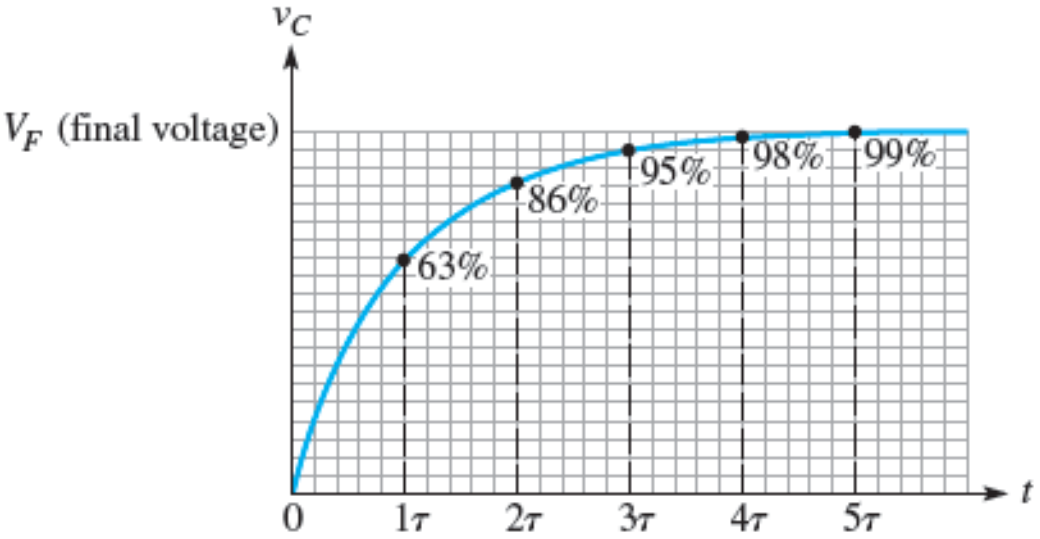


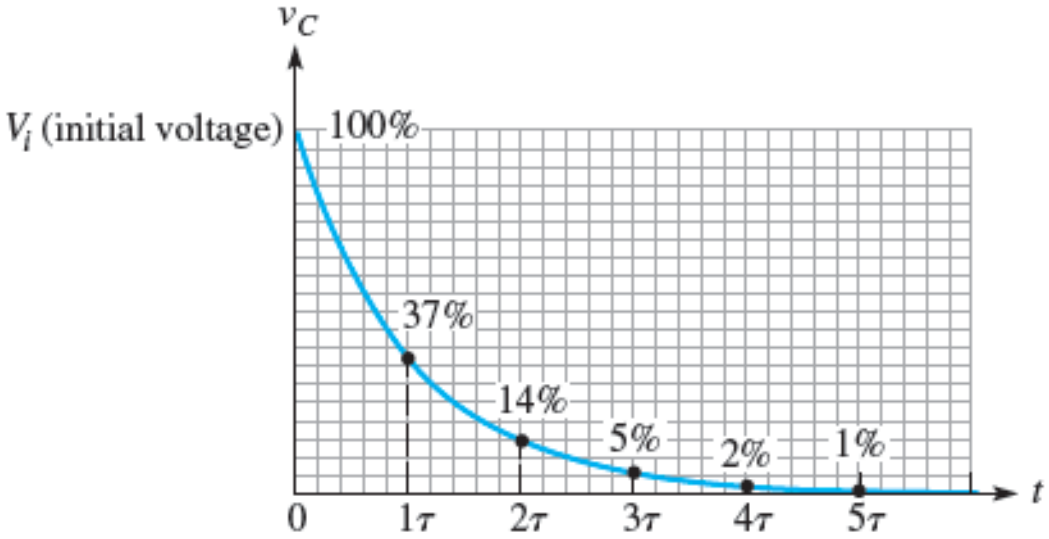
Fig. 2: Positive clamping operation with a passive clamper.

Passive diode clamping circuit

RC time constant: it is the time required to charge the capacitor, through the resistor, from an initial charge voltage of zero to approximately **63.2%** of the value of an applied DC voltage or to discharge the capacitor through the same resistor to approximately **36.8%** of its initial charge voltage. $\tau = RC$



(a) Charging curve with percentages of the final voltage



(b) Discharging curve with percentages of the initial voltage

Fig. 3: Exponential voltage curves for the charging and discharging of a capacitor in an RC circuit.

Passive diode clamping circuit

The net effect of the clamping action is that:

- The capacitor retains a charge approximately equal to the peak value of the input less the diode drop ($V_{p(in)} - 0.7$).
- The DC voltage of the capacitor adds to the input voltage by superposition.

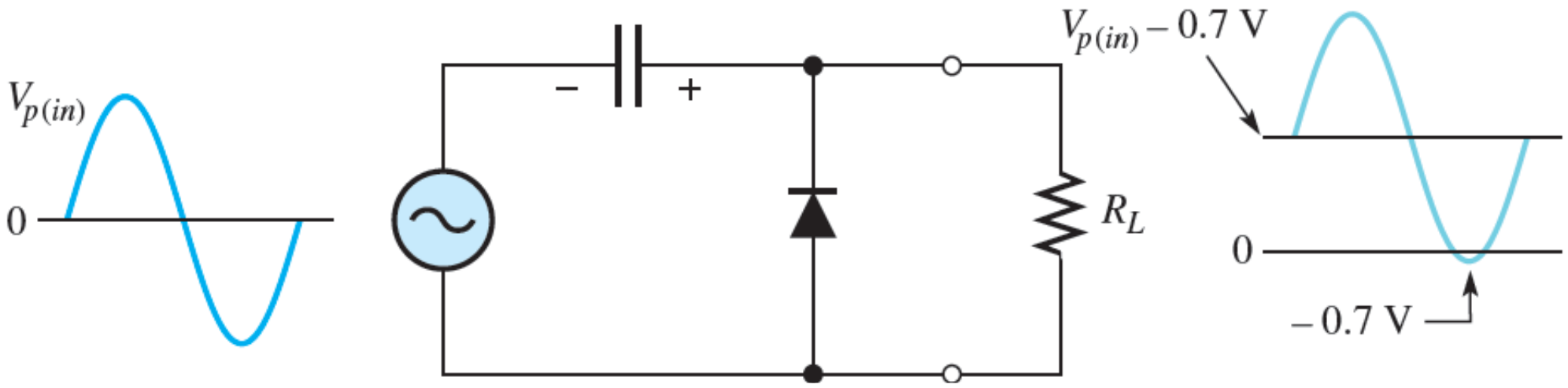


Fig. 2: Positive clamping operation with a passive clamper.

Passive diode clamping circuit

What would happen if the diode were flipped?

If the diode is turned around, a negative DC voltage is added to the input signal, as shown in Fig. 4.

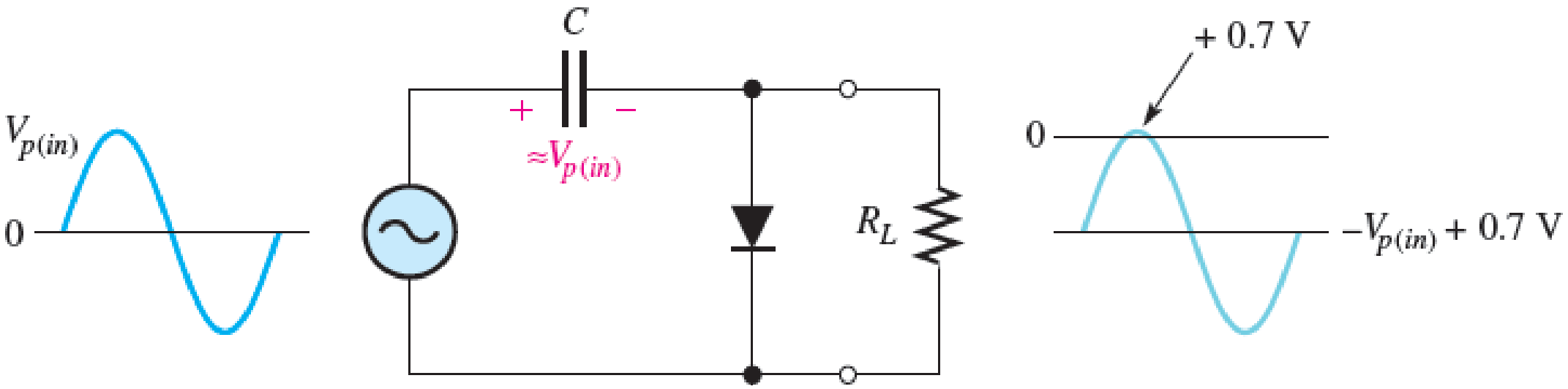


Fig. 4: Negative clamping operation with a passive clamper.

An Active Clamping Circuit

A positive clamper with an op-amp and a diode is shown in Fig. 5.

This circuit overcomes a couple of disadvantages of the passive clamper.

- The use of the op-amp eliminates the peak found in the positive passive clamper output.
- It prevents loading the input source when the diode is forward-biased.

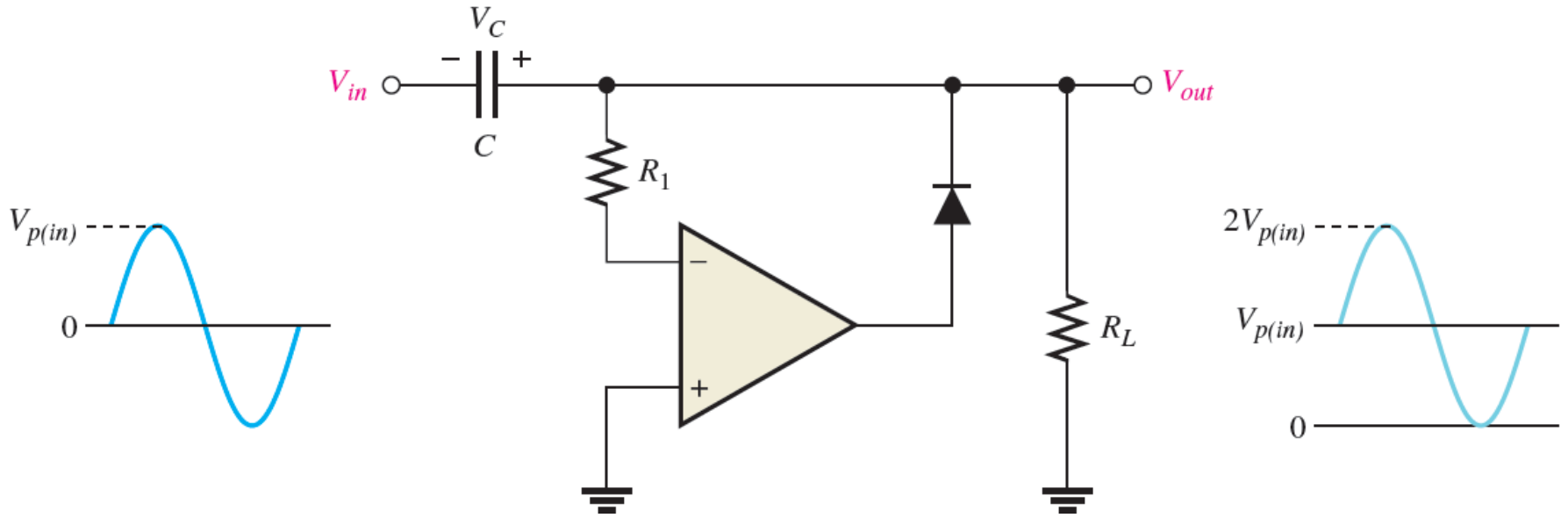


Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

On the first negative half-cycle of the input voltage V_{in}

The differential input is positive, which produces a positive output voltage. Because of the feedback loop, the positive op-amp output voltage forward-biases the diode, allowing the capacitor to charge quickly.

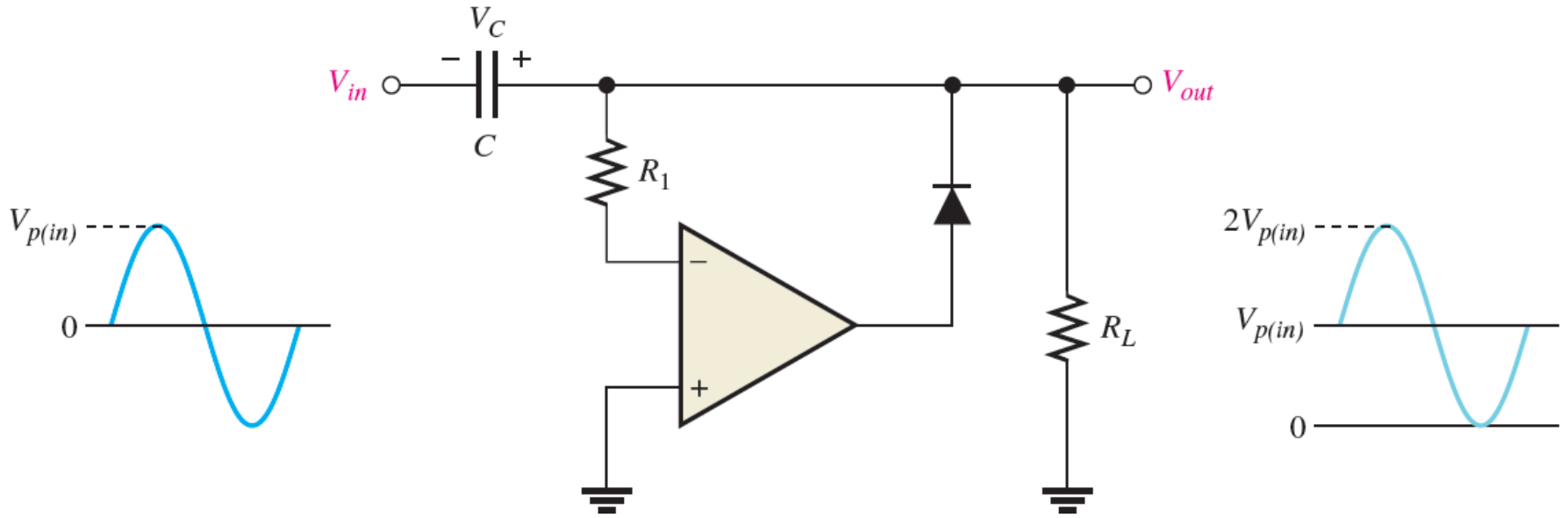


Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

On the first negative half-cycle of the input voltage V_{in}

The maximum voltage across the capacitor occurs at the negative peak of the input with the polarity shown in Fig. 5. This capacitor voltage adds to the input voltage so that the minimum peak of the output voltage, V_{out} is at 0 V, as indicated.

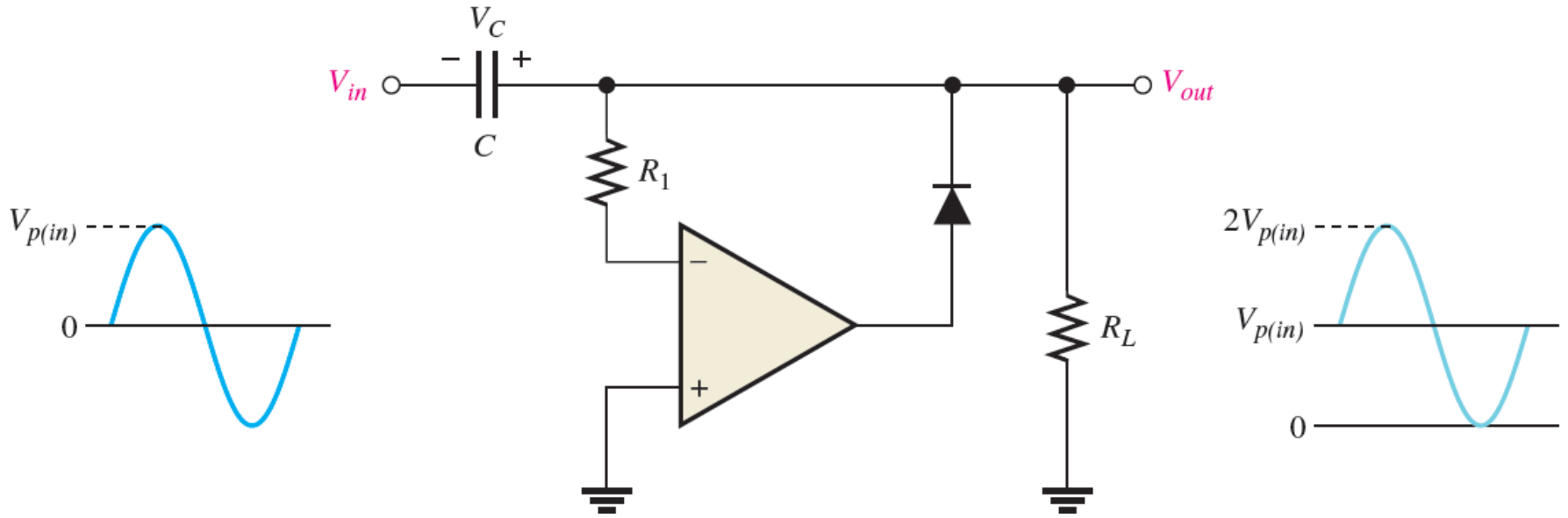


Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

During the time between the minimum output peaks of V_{out} and after the capacitor is charged, the differential input voltage to the op-amp becomes negative. As a result, the output of the op-amp becomes negative and reverse-biases the diode, thus breaking the feedback path. The only change in the capacitor voltage during this time is due to a very small discharge through R_L.

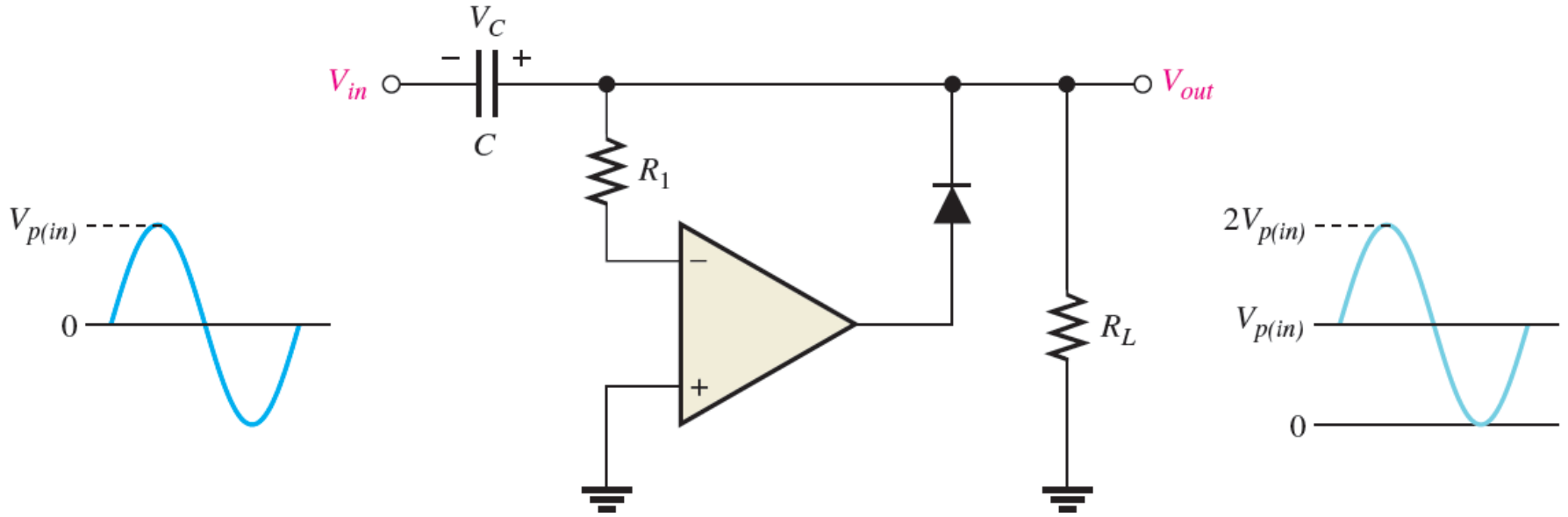


Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

At each minimum peak of the signal, the diode is forward-biased for a very short time to replenish the voltage across the capacitor.

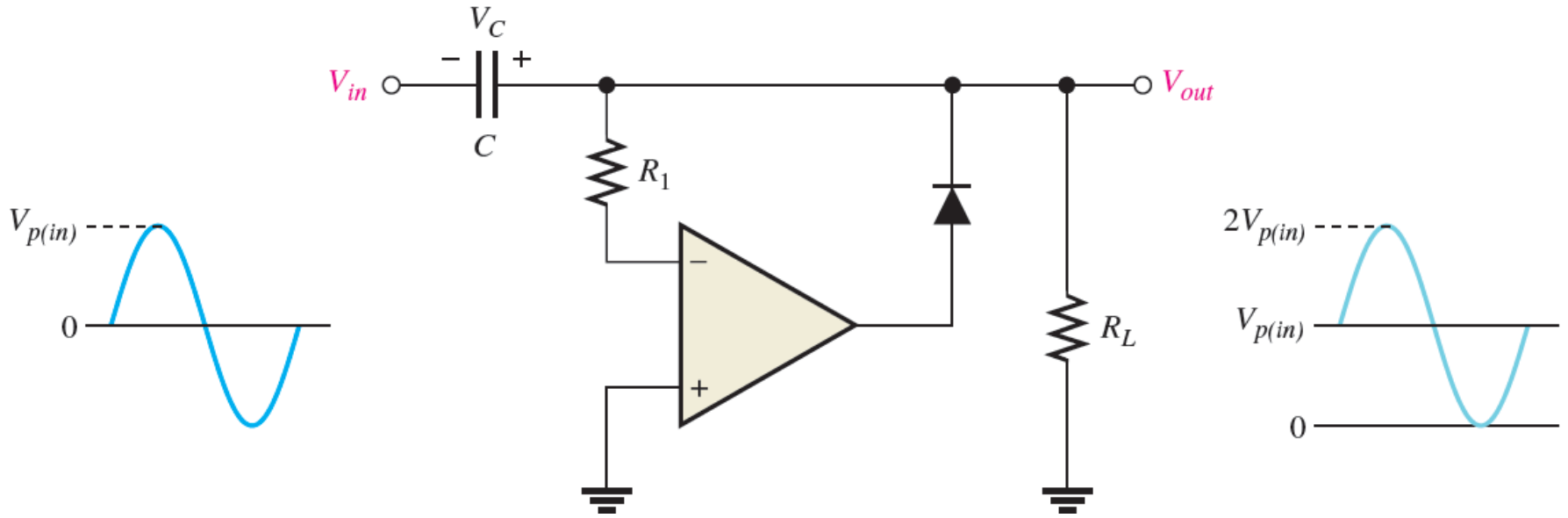


Fig. 5: An active clamping circuit and its operation.

An Active Clamping Circuit

The positive clamper can be converted to a negative clamper by reversing the diode. In this case, the output waveform would occur below 0 V with its maximum peaks at zero, as illustrated in Fig. 6

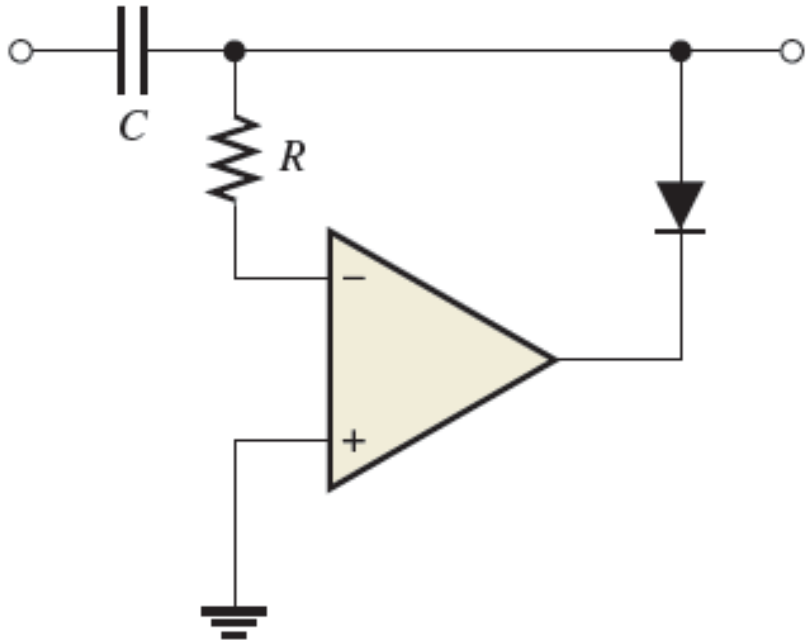


Fig. 6: Active negative clamper.

An Active Clamping Circuit

Also, the clamping level can be changed to a value other than 0 V by connecting a reference voltage source at the input of the op-amp, as shown in Fig. 7.

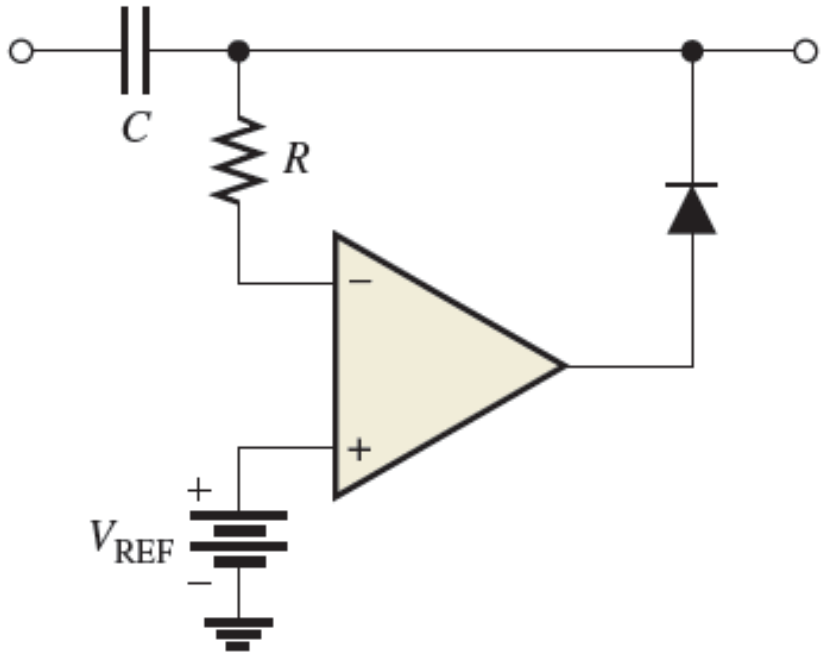


Fig. 7: Active positive clamper with nonzero reference.

An Active Clamping Circuit

Exercise: Determine the output voltage for the clamping circuit in Fig.8 for the input voltage shown.

Solution:

This is a positive clamping circuit and the reference voltage is + 1 V, so the minimum peak value of the output voltage is also +1 V. The voltage is effectively shifted by 3 V, as indicated in the figure.

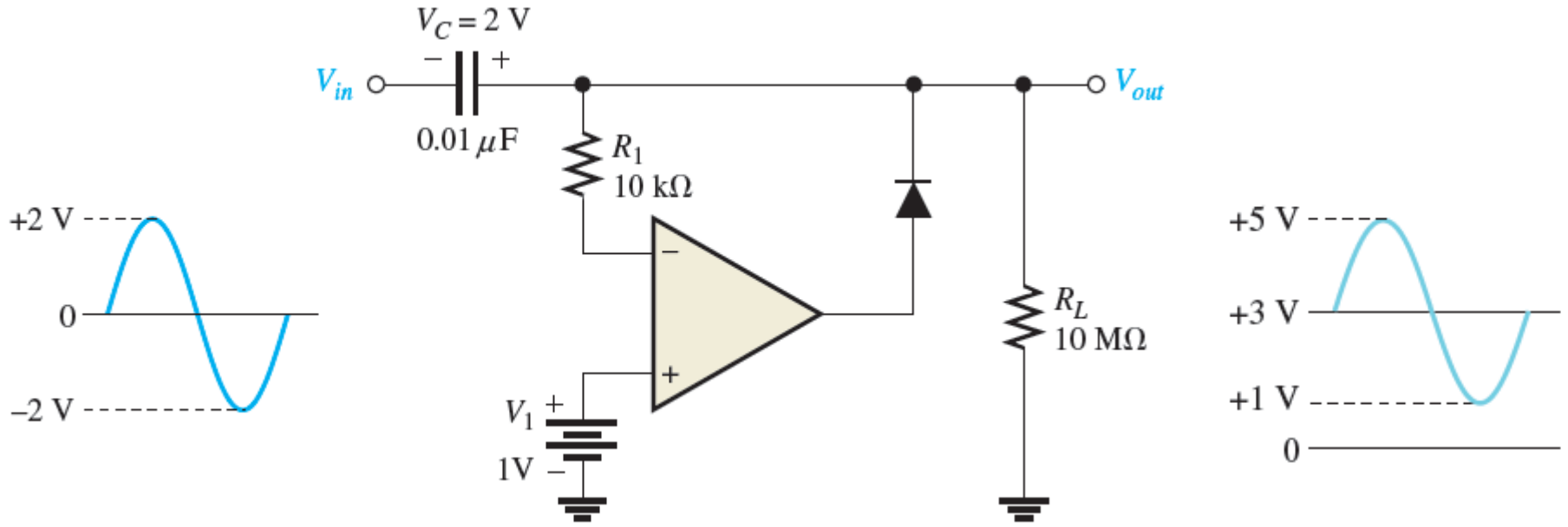


Fig. 8: Active positive clamper with nonzero reference.

An Active Clamping Circuit

Q:

a) Determine the output voltage for the clamping circuit in Fig.9 for the input voltage shown.
b) Determine the time constant for the circuit.
c) Is the clamping circuit below is sufficient if the input frequency is 100 Hz?

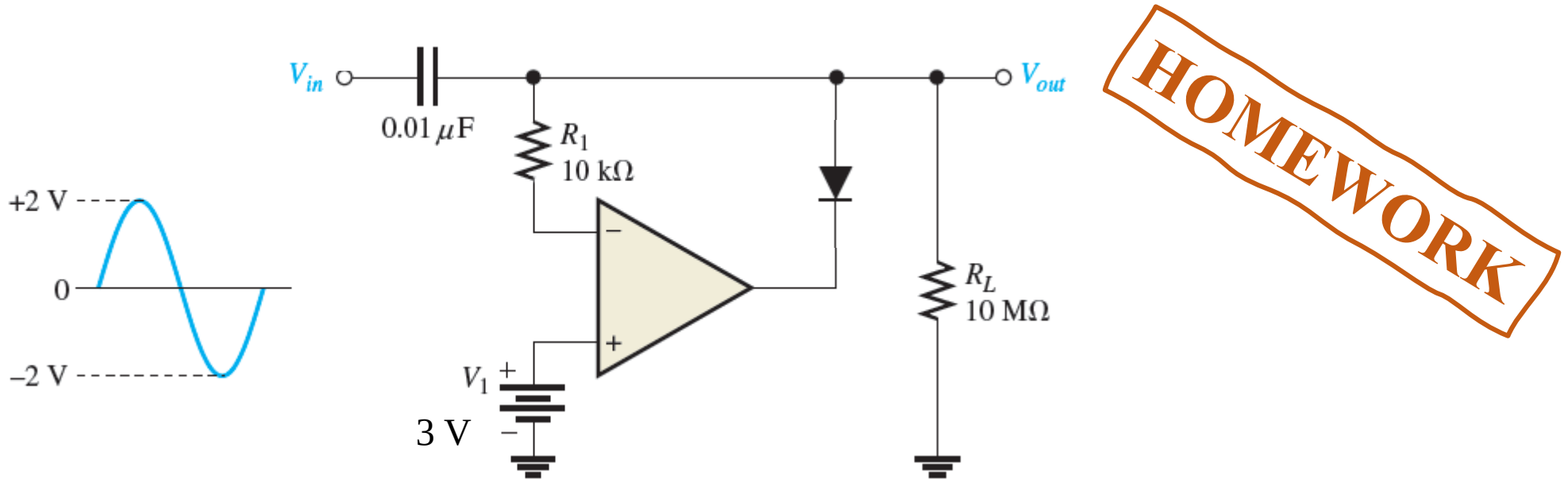


Fig. 9: Active positive clamper with nonzero reference.