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Field-Effect Transistors (FETs)

Basic Definitions:

The FET is a semiconductor device whose operation consists of controlling the flow of current through a semiconductor channel by application of an electric field (voltage).

There are two categories of FETs: the ***junction field-effect transistor*** (JFET) and the ***metal-oxide-semiconductor field-effect transistor*** (MOSFET). The MOSFET category is further broken-down into: ***depletion*** and ***enhancement*** types.

A Comparison between FET and BJT:

- FET is a ***unipolar*** device. It operates as a ***voltage-controlled*** device with either electron current in an ***n-channel*** FET or hole current in a ***p-channel*** FET.
- BJT made as ***npn*** or as ***pnp*** is a ***current-controlled*** device in which both electron current and hole current are involved.
- The FET is smaller than a BJT and is thus for more popular in ***integrated circuits*** (ICs).
- FETs exhibit much higher ***input impedance*** than BJTs.
- FETs are more ***temperature stable*** than BJTs.
- BJTs have large ***voltage gain*** than FETs when operated as an amplifier.
- The BJT has a much higher ***sensitivity*** to changes in the applied signal (faster ***response***) than a FET.

Junction Field-Effect Transistor (JFET):

The basic construction of n-channel (p-channel) JFET is shown in Fig. 15-1a (b). Note that the major part of the structure is n-type (p-type) material that forms the channel between the embedded layers of p-type (n-type) material. The top of the n-type (p-type)

channel is connected through an ohmic contact to a terminal referred to as the ***drain*** "D", while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the ***source*** "S". The two p-type materials areconnected together and to the ***gate*** "G" terminal.

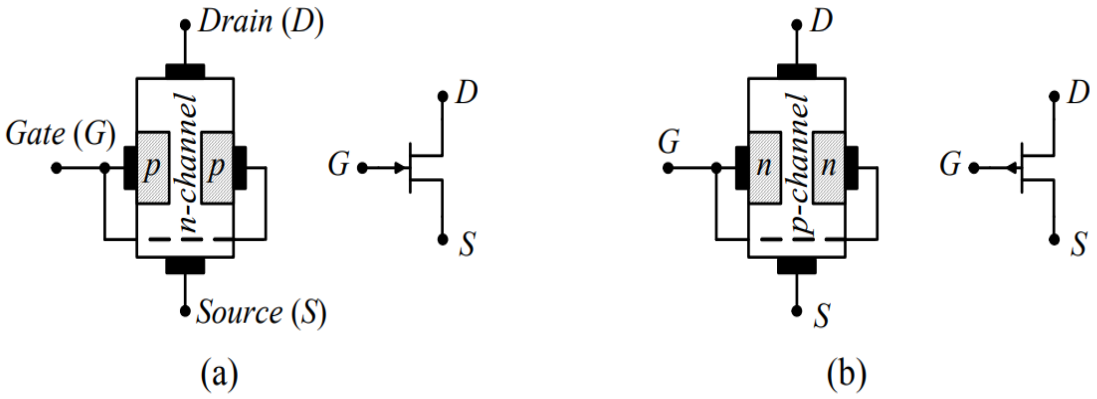


Fig. 15-1

Basic Operation of JFET:

- Bias voltages are shown, in Fig. 15-2, applied to an n-channel JFET devise.
- V_{DD} provides a drain-to-source voltage, V_{DS}, (drain is positive relative to source) and supplies current from drain to source, I_D, (electrons move from source to drain).
- V_{GG} sets the reverse-bias voltage between the gate and the source, V_{GS}, (gate is biased negative relative to the source).
- Input impedance at the gate is very high, thus the gate current $I_G = 0$ A.
- Reverse biasing of the gate-source junction produces a depletion region in the n-channel and thus increases its resistance.
- The channel width can be controlled by varying the gate voltage, and thereby, I_D can also be controlled.
- The depletion regions are wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is grater than that between the gate and the source.

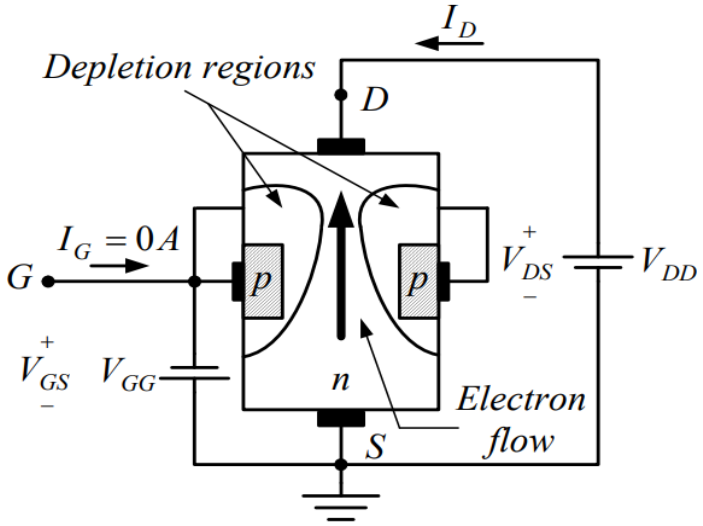


Fig. 15-2

JFET Characteristics:

◄ When $V_{GS} = 0$ V and $V_{DS} < |V_P|$ (***pinch-off voltage***)*: I_D rises linearly with V_{DS} (***ohmic region***, n-channel resistance is constant), as shown in Fig. 15-3.

* *When V_{DS} is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_P.*

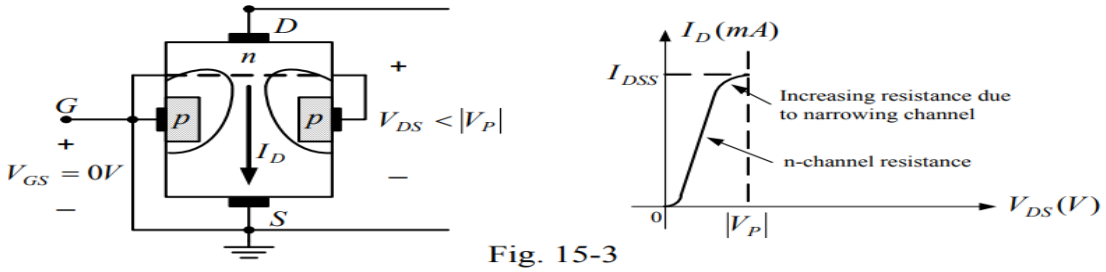


Fig. 15-3

◄ When $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$: I_D remains at its saturation value I_{DSS} beyond V_P, as shown in Fig. 15-4.

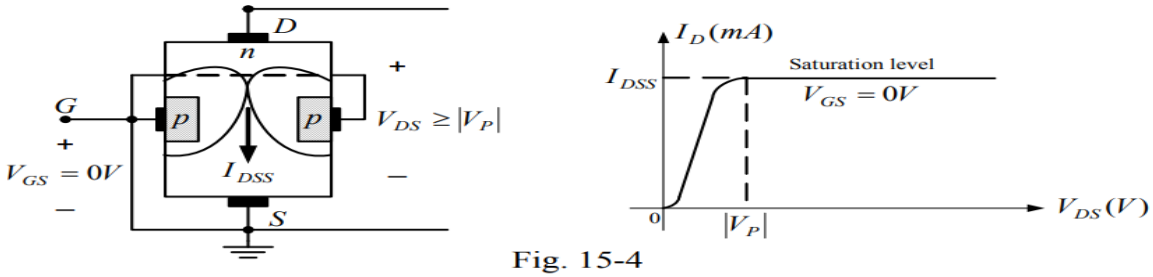


Fig. 15-4

◄ When $V_{GS} < 0$ and V_{DS} some positive value: The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at lower level of V_{DS}, as shown in Fig. 15-5.

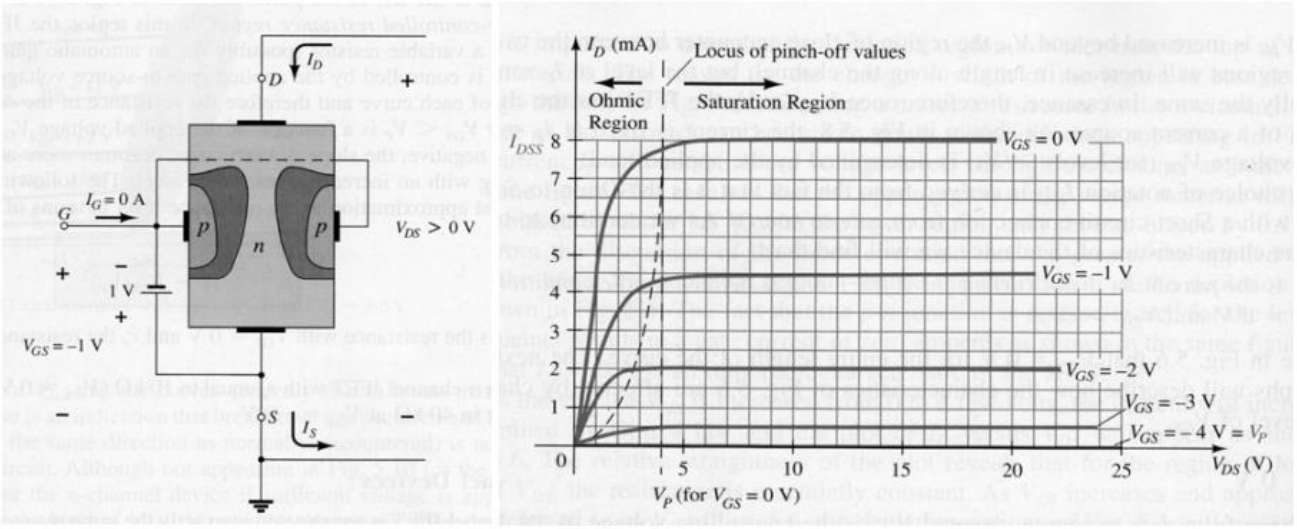


Fig. 15-5

Summary:

For n-channel JFET:

1. The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$ as shown in Fig. 15-6a.
2. For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A) as appearing in Fig. 15-6b.
3. For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as shown in Fig. 15-6c.

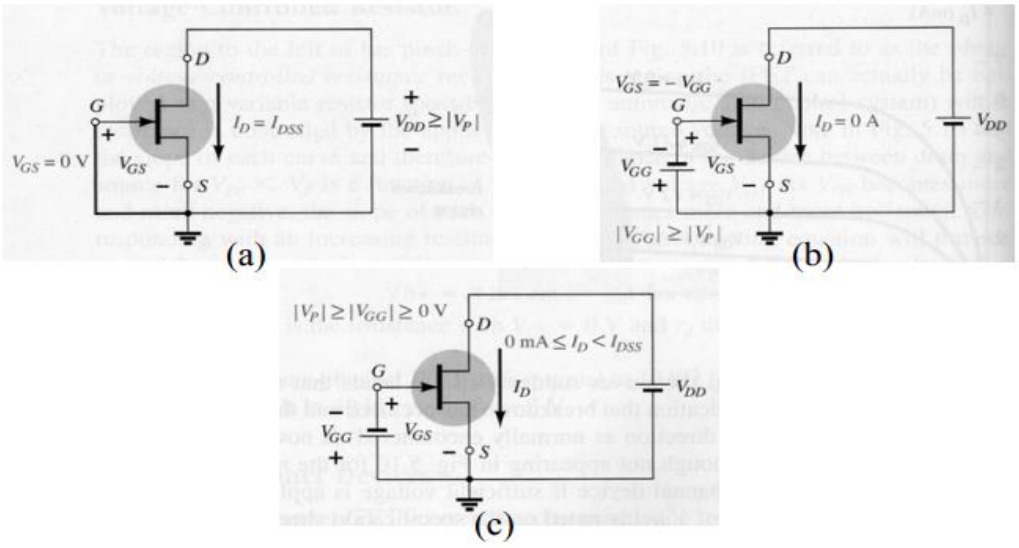


Fig. 15-6

For p-channel JFET a similar list can be developed (see Fig. 15-7).

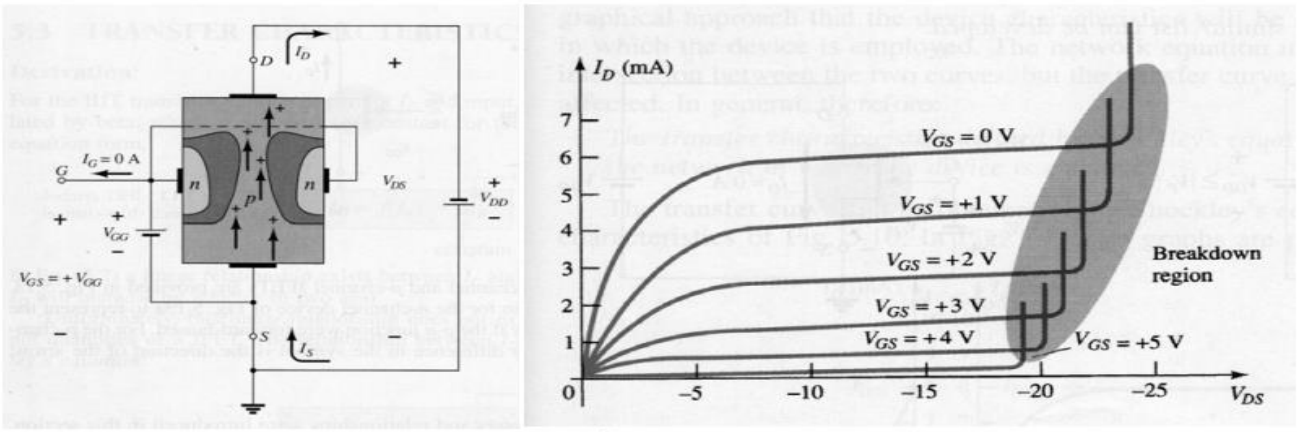


Fig. 15-7

Shockley's Equation:

For the BJT the output current I_C and input controlling current I_B were related by β, which was considered constant for the analysis to be performed. In equation form:

control variable

$$I_C = \beta \cdot I_B$$

constant

In the above equation a linear relationship exists between I_C and I_B.

Unfortunately, this linear relationship does not exist between the output (I_D) and input (V_{GS}) quantities of a JFET. The relationship between I_D and V_{GS} is defined by Shockley's equation:

control variable

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad [15.1]$$

constant

The squared term of the equation will result in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

Transfer Characteristics:

Transfer characteristics are plots of I_D versus V_{GS} for a fixed value of V_{DS}. The transfer curve can be obtained from the output characteristics as shown in Fig. 15-8, or it can be sketched to a satisfactory level of accuracy (see Fig. 15-9) simply using Shockley's equation with the four plot points defined in Table 15-1.

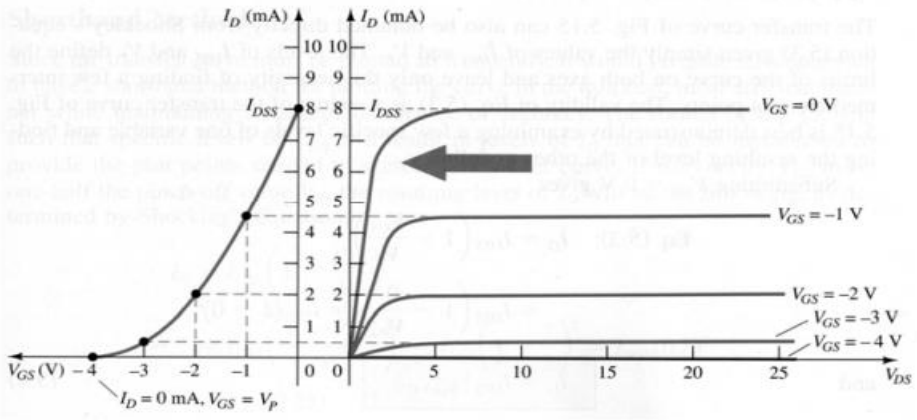


Fig. 15-8

Table 15-1

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	
V_{GS} (V)	I_D (mA)
0	I_{DSS}
0.3 V_P	I_{DSS} / 2
0.5 V_P	I_{DSS} / 4
V_P	0

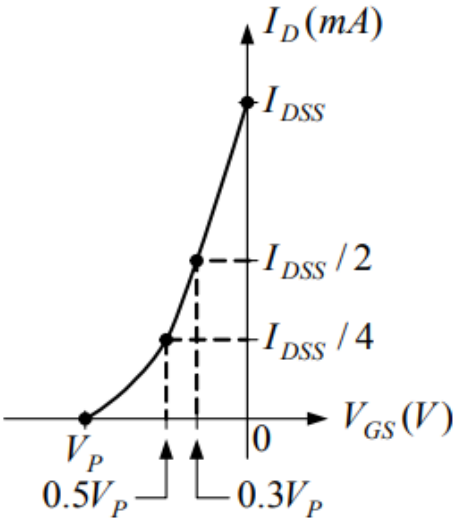
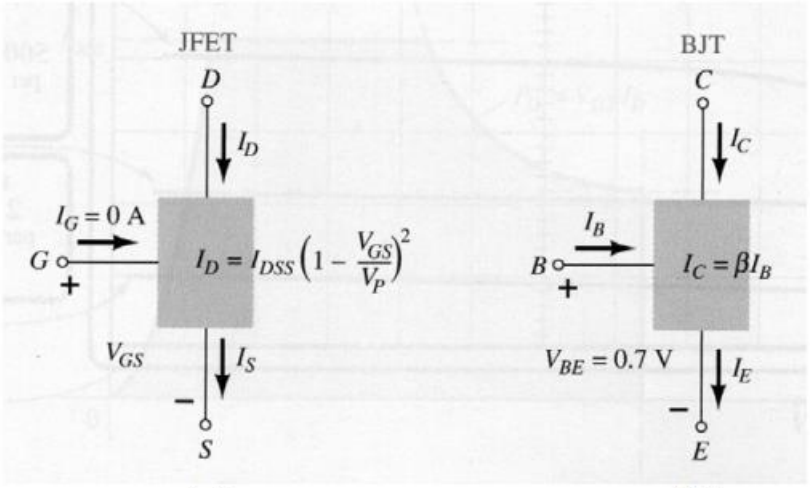


Fig. 15-9

Important Relationships:

A number of important equations and operating characteristics have introduced in the last few sections that are of particular importance for the analysis to follow for the dc and ac configurations. In an effort to isolate and emphasize their importance, they are repeated below next to a corresponding equation for the BJT. The JFET equations are defined for the configuration of Fig. 15-10a, while the BJT equations relate to Fig. 15-10b.



(a) (b)

Fig. 15-10

JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0A$	$\Leftrightarrow$	$V_{BE} \cong 0.7V$

JFET AC Equivalent Circuit

The control of I_d by V_{gs} is include as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 15-13. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will as occurin actual operation. The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source.