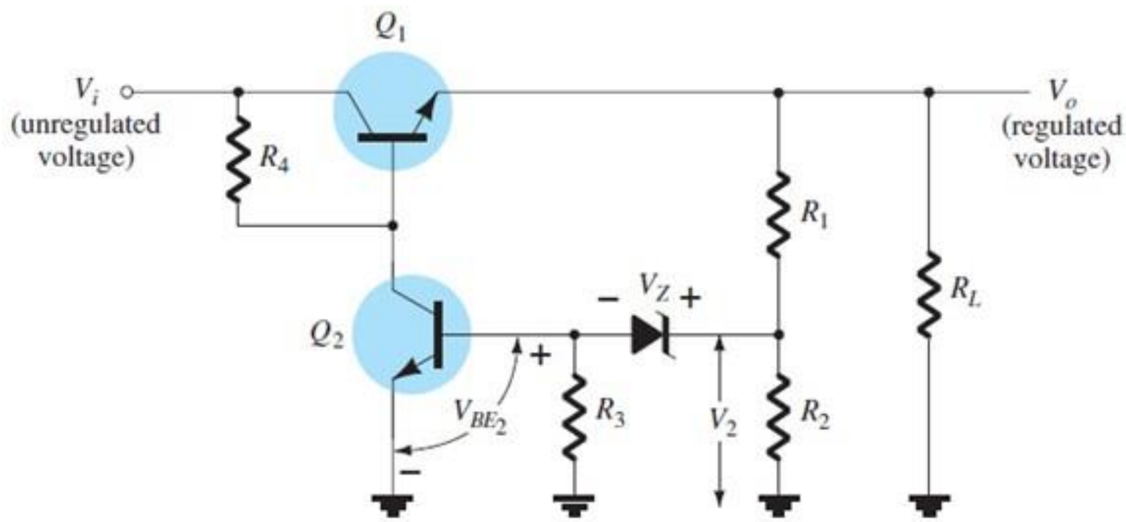
Al-Mustaqbal University College
Department of Medical Instrumentation Techniques Engineering
Class: Three
Subject: Medical electronic system
Lecturer: Dr. zahraa hashim kareem
Lecture-3: voltage series regulator

Improved Series Regulator An improved series regulator circuit is shown in Fig. 15.15 . Resistors *R* 1 and *R* 2 act as a sampling circuit, with Zener diode *D Z* providing a reference voltage, and transistor *Q* 2 then controls the base current to transistor *Q* 1 to vary the current passed by transistor *Q* 1 to maintain the output voltage constant.



Improved series regulator circuit.

If the output voltage tries to increase, the increased voltage, *V* 2 , sampled by *R* 1 and *R* 2 , causes the base-emitter voltage of transistor *Q* 2 to go up (since *V Z* remains fixed). If *Q* 2 conducts more current, less goes to the base of transistor *Q* 1 , which then passes less current to the load, reducing the output voltage— thereby maintaining the output voltage constant. The opposite takes place if the output voltage tries to decrease, causing less current to be supplied to the load, to keep the voltage from decreasing.

$$V_o = \frac{R_1 + R_2}{R_2}(V_Z + V_{BE_2})$$

EXAMPLE What regulated output voltage is provided by the circuit of Fig. for the circuit elements $R_1 = 20\ k\Omega$, $R_2 = 30\ k\Omega$, and $V_Z = 8.3$ V?

Solution: From Eq. , the regulated output voltage is

$$V_o = \frac{20\ k\Omega + 30\ k\Omega}{30\ k\Omega}(8.3\ V + 0.7\ V) = \mathbf{15\ V}$$

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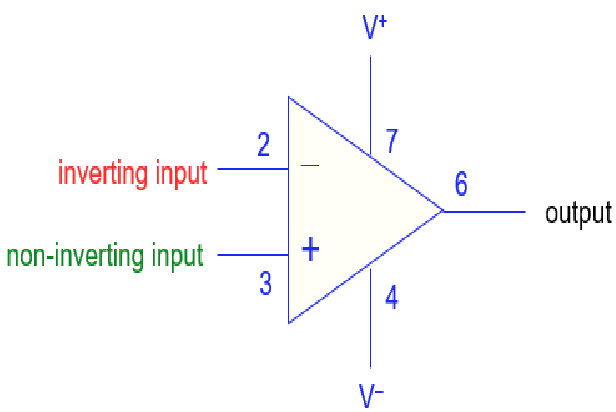
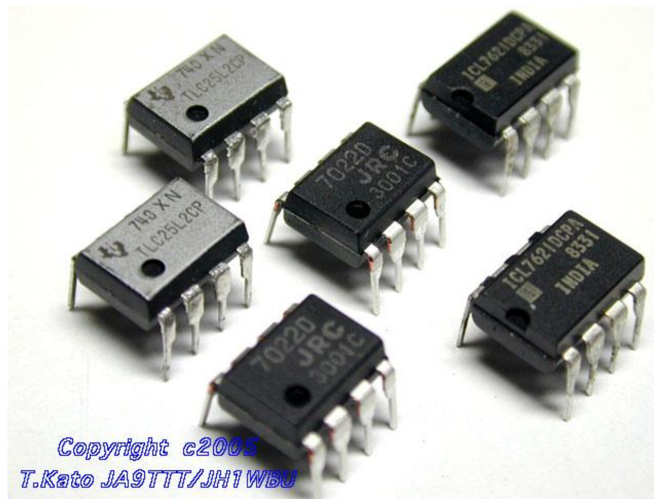
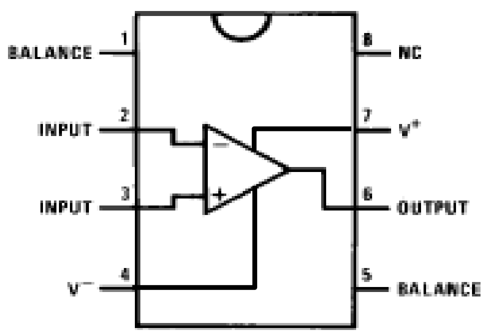
Operational Amplifiers







- Op-amps (amplifiers/buffers in general) are drawn as a triangle in a circuit schematic
- There are two inputs
  - inverting and non-inverting
- And one output
- Also power connections (note no explicit ground)

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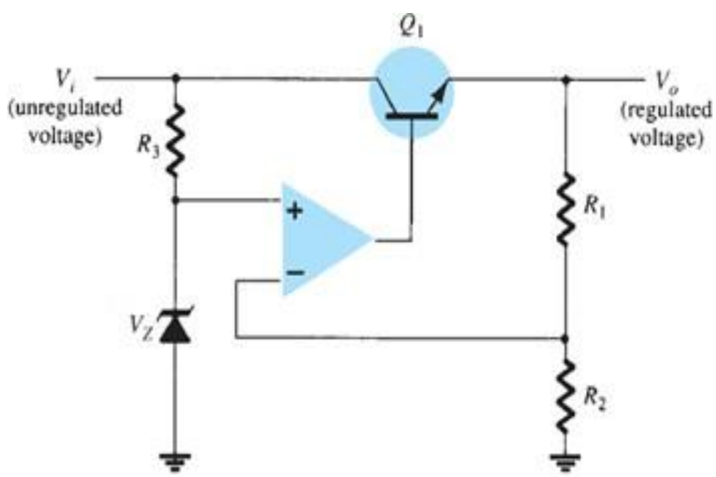
- Infinite voltage gain
  - a voltage difference at the two inputs is magnified infinitely
  - in truth, something like 200,000
  - means difference between + terminal and – terminal is amplified by 200,000!
- Infinite input impedance
  - no current flows into inputs
  - in truth, about 10^{12} Ω for FET input op-amps
- Zero output impedance
  - rock-solid independent of load
  - roughly true up to current maximum (usually 5–25 mA)
- Infinitely fast (infinite bandwidth)
  - in truth, limited to few MHz range
  - slew rate limited to 0.5–20 V/μs

Op-Amp Series Regulator Another type of series regulator is shown in Fig. The op-amp compares the Zener diode reference voltage with the feedback voltage.

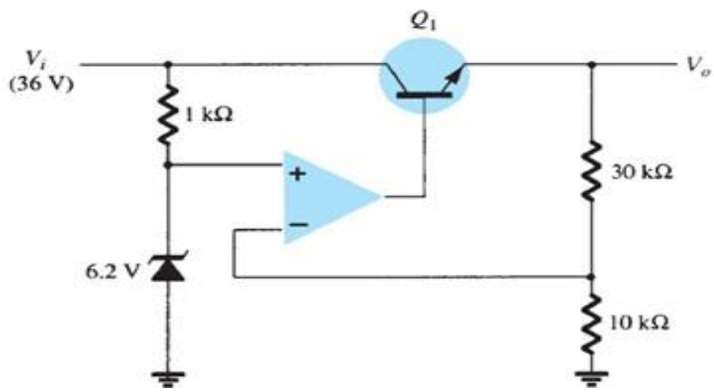
from sensing resistors R_1 and R_2. If the output voltage varies, the conduction of transistor Q_1 is controlled to maintain the output voltage constant. The output voltage will be maintained at a value of

$$V_o = \left(1 + \frac{R_1}{R_2}\right)V_Z$$



Op-amp series regulator circuit.

EXAMPLE Calculate the regulated output voltage in the circuit of Fig.



Solution:

$$V_o = \left(1 + \frac{30\ \text{k}\Omega}{10\ \text{k}\Omega}\right)6.2\ \text{V} = \mathbf{24.8\ V}$$