Al Mustaqbal University College

STUDENT NAME:	
TUTOR NAME:	**Dr. Ameer Al-khaykan**
PROGRAMME:	**Electrical Circuit**
SUBJECT:	**Electrical and Electronics**
COURSEWORK TITLE:	**Collector-Feedback Bias Transistor**

Issue Date:	Due Date:	Feedback Date:	Extension Date:

PERFORMANCE

TARGETED LEARNING OUTCOMES

4. Solve problems involving basic analogue and digital electronic circuits using numerical skills appropriate to an engineer.

5. Identify and safely use standard laboratory equipment to extract data, then apply in the solution of an electronic or electrical engineering problem;

6. Adopt a logical approach to the solution of engineering problems.

Important Information – Please Read Before Completing Your Work

All students should submit their work by the date specified using the procedures specified in the Student Handbook. An assessment that has been handed in after this deadline will be marked initially as if it had been handed in on time, but the Board of Examiners will normally apply a lateness penalty.
Your attention is drawn to the Section on Academic Misconduct in the Student's Handbook.

All work will be considered as individual unless collaboration is specifically requested, in which case this should be explicitly acknowledged by the student within their submitted material.

Any queries that you may have on the requirements of this assessment should be e-mailed to **ameer.alkhaykan@mustaqbal-college.edu.iq**
No queries will be answered after respective submission dates.
You must ensure you retain a copy of your completed work prior to submission.

MARKING CRITERIA

COURSEWORK WILL BE MARKED ACCORDING TO THE FOLLOWING UNIVERSITY CRITERIA.

90-100%: a range of marks consistent with a first where the work is exceptional in all areas;

80-89%: a range of marks consistent with a first where the work is exceptional in most areas.

70-79%: a range of marks consistent with a first. Work which shows excellent content, organisation and presentation, reasoning and originality; evidence of independent reading and thinking and a clear and authoritative grasp of theoretical positions; ability to sustain an argument, to think analytically and/or critically and to synthesise material effectively.

60-69%: a range of marks consistent with an upper second. Well-organised and lucid coverage of the main points in an answer; intelligent interpretation and confident use of evidence, examples and references; clear evidence of critical judgement in selecting, ordering and analysing content; demonstrates some ability to synthesise material and to construct responses, which reveal insight and may offer some originality.

50-59%: a range of marks consistent with lower second; shows a grasp of the main issues and uses relevant materials in a generally business-like approach, restricted evidence of additional reading; possible unevenness in structure of answers and failure to understand the more subtle points: some critical analysis and a modest degree of insight should be present.

40-49%: a range of marks which is consistent with third class; demonstrates limited understanding with no enrichment of the basic course material presented in classes; superficial lines of argument and muddled presentation; little or no attempt to relate issues to a broader framework; lower end of the range equates to a minimum falls short in one or more areas.

.

35-39%: achieves many of the learning outcomes required for a mark of 40% but falls short in one or more areas.

30-34%: a fail; may achieve some learning outcomes but falls short in most areas; shows considerable lack of understanding of basic course material and little evidence of research.

0-29%: a fail; basic factual errors of considerable magnitude showing little understanding of basic course material; falls substantially short of the learning outcomes for compensation.

Note:

- While constructing circuits all connects should be made with the power supply in the off position.
- Check power and ground connections (and other connections) **before** switch on the power.
- Make sure that the power and the ground are properly connected to all IC's before switch on the power.
- **DO NOT** strip wire ends longer than 1/4" and jam long bare ends into the breadboard holes. This will cause shorts and ruin the board.
- **DO NOT** short (connect) the power supply outputs together, i.e., do not allow the exposed wires to touch each other. This will cause permanent damage to the power supply.
- **DO NOT** connect the power supply to the breadboard with reverse polarity. This will cause the permanent chip damage.
- **DO NOT** connect an output of any gate to the output of another gate, to a switch, to power (+5V), or to ground. These situations will cause excessive currents and result in the permanent damage to the chip or chips involved.

1 Objects

To verify the voltages and currents in a collector-feedback bias circuit and to construct its Dc load line.

2 Theory:

The collector feedback bias circuit is one of the transistor biasing schemes which is commonly used because it stabilizes the Q point, which means that the Q point is independent of the value of βdc, since the collector voltage provides the bias for the base-emitter junction.

The feedback connection provides a very stable Q point by reducing the effect of variation in βdc due to variation in temperature.

By ohms law:

$$I_B = V_C - V_{BE} / R_B \qquad \text{Equation (1)}$$

$$V_C = V_{CC} - I_{CQ}R_C \qquad \text{Equation (2)}$$

$I_{BQ}=I_{CQ}/\beta dc$ Equation (3)

Substituting equations (2) and (3) in equation (1)

$I_{CQ}/\beta dc= (V_{CC}-I_{CQ}R_C-V_{BE})/R_B$

$(R_B/\beta dc)I_{CQ}+I_{CQ}R_C=V_{CC}-V_{BE}$

$I_{CQ} ((R_B/\beta dc) +R_C) =V_{CC}-V_{BE}$

Then : $I_{CQ}= (V_{CC}-V_{BE})/ (R_C+ (R_B/\beta dc))$

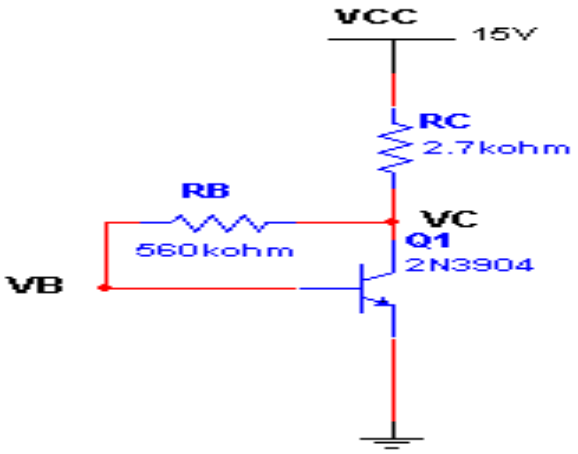

Figure (1) collector-feedback bias circuit

Note that the following relationships must be verified in the collector -feedback bias circuit:

$RC>> RB/\beta$ *and* $VCC>>VBE$

$I_{CQ}= (V_{CC}-V_{BE})/ (R_C+ (R_B/\beta))$

$I_{BQ}= (V_{CC}-V_{BE})/ (\beta R_C+R_B)$

$V_B =V_{BE}=0.7V$

$V_{CEQ} =V_{CC}-I_{CQ}R_C$

Equipment

1. 2.7 kΩ resistors
2. 560 kΩ resistor
3. 2N3904 NPN silicon transistor
4. 0-15 V dc power supply
5. Voltmeter

Procedure

1. Connect the circuit shown below in figure (1), and then switch the Dc power supply on.
2. Using the voltmeter measure **V_{BE}** and **V_{CE},** and by Ohm's law determine the quiescent collector current I_{CQ} and the quiescent base current I_{BQ}, then from these two values determine the value of **βdc** by the use of the following equation and record your results in the table No.1.

$$\beta_{dc} = I_{CQ} / I_{BQ}$$

3. Measure individually **V_B** and **V_{CEQ}** with your voltmeter and record your results in the table No.1.
4. Using the value of **V_{BE} =**0.7 V typically and the value of beta determined in step 2, calculate all the expected values of the quiescent Dc collector current **I_{CQ}**, base current **I_{BQ},** and collector to emitter voltage **V_{CEQ}** for the given collector-feedback biased circuit shown in figure (1), and then record these calculated values in the table No.1 and compare your calculated results to the measured ones.

Table No.1 (Transistor parameters)

Parameter	Measured Value	Calculated Value
I_{BQ}		
I_{CQ}		
β		
V_{BE}		
V_{CEQ}		

5.Using the equations shown below, calculate **$V_{CE(off)}$ & $I_{C(sat)}$** and record your results in table No.2, then draw the Dc load line of the collector feedback

bias transistor circuit and then plot the Q point you got on the graph, note that the Q point must locates at the Dc load line.

$$V_{CE}\ (off) = V_{CC}$$
$$I_C\ (sat) = V_{CC} / R_C$$

Table No.2 (The saturation and cut off parameters)

Parameter	Calculated value
V_{CE}(off)	
I_C(sat)	

5 Discussion

1. What are the conditions of the collector-feedback biasing circuit?
2. Why the collector-feedback biasing circuit is commonly used?
3. Compare between the collector-feedback biasing and the emitter biasing.

6 Review Questions

1. For the circuit of figure (1), if β=200, then I_C is approximately:
   (a) 2.2mA (b) 3.9mA (c) 4.8mA (d) 14.3mA

2. In the circuit of figure 1, if β of the transistor increases, then:
   (a) I_B decreases (b) I_C increases (c) V_{CE} increases
   (d) all of the above

3. The collector saturation current for the circuit of figure (1) is approximately:
   (a) 4mA (b) 6mA (c) 10mA (d) 15mA

4. At cutoff, the collector to emitter voltage for the circuit of figure (1) is:
   (a) 4V (b) 8V (c) 10V (d) 15V