Al Mustaqbal University College

STUDENT NAME:		
TUTOR NAME:	**Dr. Ameer Al-khaykan**	
PROGRAMME:	**Electrical Circuit**	
SUBJECT:	**Electrical and Electronics**	
COURSEWORK TITLE:	**JFET Transistor Characteristics**	

Issue Date:	Due Date:	Feedback Date:	Extension Date:

PERFORMANCE

TARGETED LEARNING OUTCOMES

4. Solve problems involving basic analogue and digital electronic circuits using numerical skills appropriate to an engineer.

5. Identify and safely use standard laboratory equipment to extract data, then apply in the solution of an electronic or electrical engineering problem;

6. Adopt a logical approach to the solution of engineering problems.

Important Information – Please Read Before Completing Your Work

All students should submit their work by the date specified using the procedures specified in the Student Handbook. An assessment that has been handed in after this deadline will be marked initially as if it had been handed in on time, but the Board of Examiners will normally apply a lateness penalty.
Your attention is drawn to the Section on Academic Misconduct in the Student's Handbook.

All work will be considered as individual unless collaboration is specifically requested, in which case this should be explicitly acknowledged by the student within their submitted material.

Any queries that you may have on the requirements of this assessment should be e-mailed to **ameer.alkhaykan@mustaqbal-college.edu.iq**
No queries will be answered after respective submission dates.
You must ensure you retain a copy of your completed work prior to submission.

MARKING CRITERIA

COURSEWORK WILL BE MARKED ACCORDING TO THE FOLLOWING UNIVERSITY CRITERIA.

90-100%: a range of marks consistent with a first where the work is exceptional in all areas;

80-89%: a range of marks consistent with a first where the work is exceptional in most areas.

70-79%: a range of marks consistent with a first. Work which shows excellent content, organisation and presentation, reasoning and originality; evidence of independent reading and thinking and a clear and authoritative grasp of theoretical positions; ability to sustain an argument, to think analytically and/or critically and to synthesise material effectively.

60-69%: a range of marks consistent with an upper second. Well-organised and lucid coverage of the main points in an answer; intelligent interpretation and confident use of evidence, examples and references; clear evidence of critical judgement in selecting, ordering and analysing content; demonstrates some ability to synthesise material and to construct responses, which reveal insight and may offer some originality.

50-59%: a range of marks consistent with lower second; shows a grasp of the main issues and uses relevant materials in a generally business-like approach, restricted evidence of additional reading; possible unevenness in structure of answers and failure to understand the more subtle points: some critical analysis and a modest degree of insight should be present.

40-49%: a range of marks which is consistent with third class; demonstrates limited understanding with no enrichment of the basic course material presented in classes; superficial lines of argument and muddled presentation; little or no attempt to relate issues to a broader framework; lower end of the range equates to a minimum falls short in one or more areas.

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35-39%: achieves many of the learning outcomes required for a mark of 40% but falls short in one or more areas.

30-34%: a fail; may achieve some learning outcomes but falls short in most areas; shows considerable lack of understanding of basic course material and little evidence of research.

0-29%: a fail; basic factual errors of considerable magnitude showing little understanding of basic course material; falls substantially short of the learning outcomes for compensation.

Note:

- While constructing circuits all connects should be made with the power supply in the off position.
- Check power and ground connections (and other connections) **before** switch on the power.
- Make sure that the power and the ground are properly connected to all IC's before switch on the power.
- **DO NOT** strip wire ends longer than 1/4" and jam long bare ends into the breadboard holes. This will cause shorts and ruin the board.
- **DO NOT** short (connect) the power supply outputs together, i.e., do not allow the exposed wires to touch each other. This will cause permanent damage to the power supply.
- **DO NOT** connect the power supply to the breadboard with reverse polarity. This will cause the permanent chip damage.
- **DO NOT** connect an output of any gate to the output of another gate, to a switch, to power (+5V), or to ground. These situations will cause excessive currents and result in the permanent damage to the chip or chips involved.

.1 Objects

The objective of this experiment is to show the using of the JFET Transistor and examines the characteristics of the silicon one, the relationship between I_{DSS}, and V_{GS}, the way of current flow and compares it with resistor, show that the Transistor is nonlinear device and the voltage drop in resistor.

.2 Theory:

The FET is a voltage –controlled device that uses an electrostatic field to control current. The FET begins with doped piece of silicon called a channel .on one end of the channel is a terminal called the source and on the other end of the channel is a terminal called the drain. Current in the channel is controlled by a voltage applied to a third terminal called the gate. The field effect transistors are classified as either junction gate (JFET) or insulated gate (IGFET) devices. The JFET has a reverse biased diode at the gate whereas the IGFET uses a thin glass insulting layer. Since the gate circuit of either type of FET draws almost no current, the input resistance is extremely high. Both types have similar Ac characteristics but differ in biasing methods. The gate of a JFET is made of the opposite type of material than the

channel, forming a pn junction between the gate and channel. Application of a reverse bias on these junction decreases the conductivity of the channel, reducing the source drain current. The gate diode should never be forward biased. The JFET comes in two forms: n-channel and p-channel.the junction field effect transistor shown in figure (1) and the circuit of JFET is shown in figure (2).

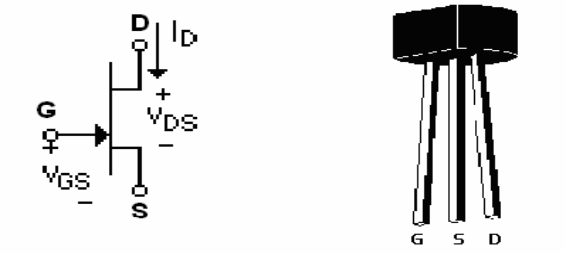

Figure (1): The Junction Field Effect Transistor.

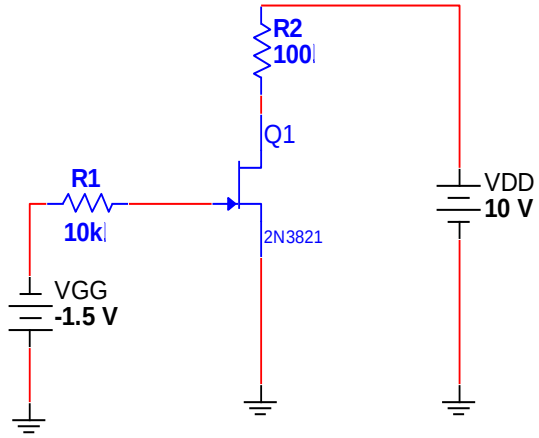

Figure (2) JFET circuit

10.3 Equipment

1. Variable DC power supply
2. Voltmeter
3. 2N3821A JFET Transistor
4. 10 KΩ, 100 Ω Resistors
5. Oscilloscope

.4 Procedure

1. Measure and record the value of the resistors in table (1) .R_1 is used for protection in case the JFET Is forward –biased .R_2 serves as a current sensing resistor.

Table (1) (The value of resistors)

2. Connect the circuit shown in figure (2).start with V_{GG} And V_{DD} at 0V, connect a voltmeter between the drain and source.

3. Keep V_{GG} at 0V and slowly increase V_{DD} until V_{DS} is 1v.

4. With V_{DS} at 1v, measure the voltage across R_2 (V_{R2}).compute the drain current I_D by applying ohms law to R_2.note that the current in R2 is the same as I_D for the transistor. Use the measured voltage V_{R2} and the measured resistance R2 to determine I_D.

5. Adjust V_{GG} for all the value in the table (2) and measure V_{R2} and I_D as before.

Table (2) (Data of drain characteristics curve for JFET transistor)

Gate voltage	V_{R2}(measured)	I_D (calculated)
0v		
-0.5v		
-1v		
-1.5v		

Resistor	Listed value	Measured value
R_1	10 KΩ	
R_2	100 Ω	

.5 Discussion

1. Compare between BJT and JFET (in terms of characteristics, applications).
2. Why should a JFET be operated with only reverse bias on the gate source?
3. What are the types of the JFET and explain about the type's structure?

.6 Review Questions

1. The field effect transistor is a:
    a) Voltage controlled device.
    b) Current controlled device.
    c) All the above
2. Current in the channel of FET is controlled by a voltage applied to the:
    a) Gate.
    b) Source.
    c) Gate and source.
3. Field effect transistors are classified to:
    a) N channel and p channel.
    b) JFET and IGFET.
    c) NPN and PNP.
4. The gate of a JFET is made of:
    a) The same type of the channel material.
    b) The opposite type of material than the channel.
    c) Thin glass –insulting layer.