

## Al Mustaqbal University College



| Student <br> NAmE: |  |  |
| :--- | :--- | :--- |
| Tutor Name: | Dr. Ameer Al-khaykan |  |
| Programme: | Electrical Circuit |  |
| Subject: | Electrical and Electronics |  |
| Coursework <br> Time: | $\Delta$-Y and Y-- Circuit Conversions |  |


| Issue Date: | Due Date: | Feedback Date: |
| :--- | :--- | :--- |
| PERtension Date: |  |  |
|  | TARGETED LEARNING OUTCOMES |  |

4. Solve problems involving basic analogue and digital electronic circuits using numerical skills appropriate to an engineer.
5. Identify and safely use standard laboratory equipment to extract data, then apply in the solution of an electronic or electrical engineering problem;
6. Adopt a logical approach to the solution of engineering problems.

# Important Information - Please Read Before Completing Your Work 

All students should submit their work by the date specified using the procedures specified in the Student Handbook. An assessment that has been handed in after this deadline will be marked initially as if it had been handed in on time, but the Board of Examiners will normally apply a lateness penalty.

Your attention is drawn to the Section on Academic Misconduct in the Student's Handbook.
All work will be considered as individual unless collaboration is specifically requested, in which case this should be explicitly acknowledged by the student within their submitted material.

Any queries that you may have on the requirements of this assessment should be e-mailed to ameer.alkhaykan@mustaqbal-college.edu.iq
No queries will be answered after respective submission dates.
You must ensure you retain a copy of your completed work prior to submission.

## MARKING CRITERIA

## Coursework will be marked according to the following university criteria.

90-100\%: a range of marks consistent with a first where the work is exceptional in all areas;
80-89\%: a range of marks consistent with a first where the work is exceptional in most areas.

70-79\%: a range of marks consistent with a first. Work which shows excellent content, organisation and presentation, reasoning and originality; evidence of independent reading and thinking and a clear and authoritative grasp of theoretical positions; ability to sustain an argument, to think analytically and/or critically and to synthesise material effectively.

60-69\%: a range of marks consistent with an upper second. Well-organised and lucid coverage of the main points in an answer; intelligent interpretation and confident use of evidence, examples and references; clear evidence of critical judgement in selecting, ordering and analysing content; demonstrates some ability to synthesise material and to construct responses, which reveal insight and may offer some originality.

50-59\%: a range of marks consistent with lower second; shows a grasp of the main issues and uses relevant materials in a generally business-like approach, restricted evidence of additional reading; possible unevenness in structure of answers and failure to understand the more subtle points: some critical analysis and a modest degree of insight should be present.

40-49\%: a range of marks which is consistent with third class; demonstrates limited understanding with no enrichment of the basic course material presented in classes; superficial lines of argument and muddled presentation; little or no attempt to relate issues to a broader framework; lower end of the range equates to a minimum falls short in one or more areas.

35-39\%: achieves many of the learning outcomes required for a mark of $40 \%$ but falls short in one or more areas.

30-34\%: a fail; may achieve some learning outcomes but falls short in most areas; shows considerable lack of understanding of basic course material and little evidence of research.
$\mathbf{0 - 2 9 \%}$ : a fail; basic factual errors of considerable magnitude showing little understanding of basic course material; falls substantially short of the learning outcomes for compensation.

## Note:

- While constructing circuits all connects should be made with the power supply in the off position.
- Check power and ground connections (and other connections) before switch on the power.
- Make sure that the power and the ground are properly connected to all IC's before switch on the power.
- DO NOT strip wire ends longer than $1 / 4^{\prime \prime}$ and jam long bare ends into the breadboard holes. This will cause shorts and ruin the board.
- DO NOT short (connect) the power supply outputs together, i.e., do not allow the exposed wires to touch each other. This will cause permanent damage to the power supply.
- DO NOT connect the power supply to the breadboard with reverse polarity. This will cause the permanent chip damage.
- DO NOT connect an output of any gate to the output of another gate, to a switch, to power $(+5 \mathrm{~V})$, or to ground. These situations will cause excessive currents and result in the permanent damage to the chip or chips involve.


## 1. Objects:

1. To verify $\Delta-Y$ and $Y-\Delta$ circuit conversions practically.

## 2. Apparatus:

- Multimeter.
- Number of resistors.
- D.C. power supply.


## 3. Theory:

Consider the resistors $R_{a}, R_{b}$ and $R_{c}$ which are connected in $\Delta$, Fig. (3-1a), the equivalent Y connected resistors must satisfy the condition that the total resistance between any two terminals in one configuration must be equal to that in the second configuration. Consider the Y configuration shown in Fig. (3-1b) From Fig. (3-1a):

$$
\begin{equation*}
R_{a b}=\frac{R_{c}\left(R_{a}+R_{b}\right)}{R_{a}+R_{b}+R_{c}} \tag{3.1}
\end{equation*}
$$

From Fig. (3-1b):

$$
\begin{equation*}
\mathrm{R}_{\mathrm{ab}}=\mathrm{R}_{1}+\mathrm{R}_{2} . \tag{3.2}
\end{equation*}
$$

The following condition must apply:
$\mathrm{R}_{1}+\mathrm{R}_{2}=\frac{\mathrm{R}_{\mathrm{c}}\left(\mathrm{R}_{\mathrm{a}}+\mathrm{R}_{\mathrm{b}}\right)}{\mathrm{R}_{\mathrm{a}}+\mathrm{R}_{\mathrm{b}}+\mathrm{R}_{\mathrm{c}}}$.
Similarly for $R_{a c}$ :
$\mathrm{R}_{1}+\mathrm{R}_{3}=\frac{\mathrm{R}_{\mathrm{b}}\left(\mathrm{R}_{\mathrm{a}}+\mathrm{R}_{\mathrm{c}}\right)}{\mathrm{R}_{\mathrm{a}}+\mathrm{R}_{\mathrm{b}}+\mathrm{R}_{\mathrm{c}}}$.
And for $R_{b c}$ :
$R_{2}+R_{3}=\frac{R_{a}\left(R_{b}+R_{c}\right)}{R_{a}+R_{b}+R_{c}}$.

Solving equations (3.3), (3.4) and (3.5) for the unknowns, $R_{1}, R_{2}$ and $R_{3}$ in terms of $R_{a}, R_{b}$ and $R_{c}$ yields:

$$
\begin{align*}
& R_{1}=\frac{R_{b} R_{c}}{R_{a}+R_{b}+R_{c}} .  \tag{3.6}\\
& R_{2}=\frac{R_{a} R_{c}}{R_{a}+R_{b}+R_{c}} .  \tag{3.7}\\
& R_{3}=\frac{R_{a} R_{b}}{R_{a}+R_{b}+R_{c}} .
\end{align*}
$$

Or solving the same equations (3.3), (3.4) and (3.5) for the unknowns $R_{a}, R_{b}$ and $R_{c}$ in terms of $R_{1}, R_{2}$ and $R_{3}$ yields:

$$
\begin{equation*}
\mathrm{R}_{\mathrm{a}}=\frac{\mathrm{R}_{1} \mathrm{R}_{2}+\mathrm{R}_{1} \mathrm{R}_{3}+\mathrm{R}_{2} \mathrm{R}_{3}}{\mathrm{R}_{1}} \ldots \tag{3.9}
\end{equation*}
$$

$R_{b}=\frac{R_{1} R_{2}+R_{1} R_{3}+R_{2} R_{3}}{R_{2}}$.
$R_{c}=\frac{R_{1} R_{2}+R_{1} R_{3}+R_{2} R_{3}}{R_{3}}$.

## .4. Procedure:

1. Connect the circuit of Fig. (3-2).
2. Measure the current in each branch.
3. Measure the voltage across $a b, a c$ and $b c$.
4. Disconnect from the supply and measure $R_{a b}, R_{a c}$ and $R_{b c}$.
5. Calculate the equivalent $R_{1}, R_{2}$ and $R_{3}$ and connect the Y equivalent.
6. Repeat steps 2,3 and 4 above.

## 5. Discussions:

1. Check your measurements of the currents and voltages with Kirchhoff's laws.
2. Verify that the total power consumed in the $\Delta$ connected resistances is equal to that consumed by the $Y$ connected resistances.
3. Compare your measurements of currents, voltages with the calculated values of the same parameters and discuss it.

## 6. Homework

1. In Fig. (3-1a) if $R_{a}=100 \Omega, R_{b}=150 \Omega$ and $R_{c}=200 \Omega$. Calculate the value of, $R_{1}, R_{2}$ and $R_{3}$ in the equivalent Y configuration.
2. In Fig. (3-1b) if $R_{1}=33 \Omega, R_{2}=47 \Omega$ and $R_{3}=68 \Omega$ Calculate the value of, $R_{a}, R_{b}$ and $R_{c}$ in the equivalent $\Delta$ configuration.
3. Calculate the equivalent resistance of the circuit shown in Fig. (3-4).

(a)

(b)


Fig. (3-2)


Fig. (3-3)


Fig. (3-4)

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