AL MUSTAQBAL UNIVERSITY COLLEGE

STUDENT NAME:	
TUTOR NAME:	**Dr. Ameer Al-khaykan**
PROGRAMME:	Electrical Circuit
SUBJECT:	Electrical and Electronics
COURSEWORK TITLE:	Kirchhoff`s law

Issue Date:	Due Date:	Feedback Date:	Extension Date:

PERFORMANCE CRITERIA:

TARGETED LEARNING OUTCOMES

4. Solve problems involving basic analogue and digital electronic circuits using numerical skills appropriate to an engineer.

5. Identify and safely use standard laboratory equipment to extract data, then apply in the solution of an electronic or electrical engineering problem;

6. Adopt a logical approach to the solution of engineering problems.

Important Information – Please Read Before Completing Your Work

All students should submit their work by the date specified using the procedures specified in the Student Handbook. An assessment that has been handed in after this deadline will be marked initially as if it had been handed in on time, but the Board of Examiners will normally apply a lateness penalty.

Your attention is drawn to the Section on Academic Misconduct in the Student's Handbook.

All work will be considered as individual unless collaboration is specifically requested, in which case this should be explicitly acknowledged by the student within their submitted material.

Any queries that you may have on the requirements of this assessment should be e-mailed to dr.ameer
No queries will be answered after respective submission dates.

You must ensure you retain a copy of your completed work prior to submission.

MARKING CRITERIA

COURSEWORK WILL BE MARKED ACCORDING TO THE FOLLOWING UNIVERSITY CRITERIA.

90-100%: a range of marks consistent with a first where the work is exceptional in all areas;

80-89%: a range of marks consistent with a first where the work is exceptional in most areas.

70-79%: a range of marks consistent with a first. Work which shows excellent content, organisation and presentation, reasoning and originality; evidence of independent reading and thinking and a clear and authoritative grasp of theoretical positions; ability to sustain an argument, to think analytically and/or critically and to synthesise material effectively.

60-69%: a range of marks consistent with an upper second. Well-organised and lucid coverage of the main points in an answer; intelligent interpretation and confident use of evidence, examples and references; clear evidence of critical judgement in selecting, ordering and analysing content; demonstrates some ability to synthesise material and to construct responses, which reveal insight and may offer some originality.

50-59%: a range of marks consistent with lower second; shows a grasp of the main issues and uses relevant materials in a generally business-like approach, restricted evidence of additional reading; possible unevenness in structure of answers and failure to understand the more subtle points: some critical analysis and a modest degree of insight should be present.

40-49%: a range of marks which is consistent with third class; demonstrates limited understanding with no enrichment of the basic course material presented in classes; superficial lines of argument and muddled presentation; little or no attempt to relate issues to a broader framework; lower end of the range equates to a minimum falls short in one or more areas.

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35-39%: achieves many of the learning outcomes required for a mark of 40% but falls short in one or more areas.

30-34%: a fail; may achieve some learning outcomes but falls short in most areas; shows considerable lack of understanding of basic course material and little evidence of research.

0-29%: a fail; basic factual errors of considerable magnitude showing little understanding of basic course material; falls substantially short of the learning outcomes for compensation.

Note:

- While constructing circuits all connects should be made with the power supply in the off position.
- Check power and ground connections (and other connections) **before** switch on the power.
- Make sure that the power and the ground are properly connected to all IC's before switch on the power.
- **DO NOT** strip wire ends longer than 1/4" and jam long bare ends into the breadboard holes. This will cause shorts and ruin the board.
- **DO NOT** short (connect) the power supply outputs together, i.e., do not allow the exposed wires to touch each other. This will cause permanent damage to the power supply.
- **DO NOT** connect the power supply to the breadboard with reverse polarity. This will cause the permanent chip damage.
- **DO NOT** connect an output of any gate to the output of another gate, to a switch, to power (+5V), or to ground. These situations will cause excessive currents and result in the permanent damage to the chip or chips involved.

2.1. Object:.

- To verify Kirchhoff's current and voltage laws experimentally.

2.2. Apparatus

Resistors (different rating)

(DC) power supply

Measuring instruments (Ammeter, Voltmeter, Ohmmeter)

Connecting wires and board

2.3. Theory:

Thus far we have considered Ohm's law (Exp. No1) and how it may be used to find current, voltage and power associated with a resistor. However, Ohm's law by itself cannot be used to analyze even the simplest circuit. Two laws first stated by the German physicist Gustav Kirchhoff

(1824-1887) in 1847, formally known as Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL). Together with the terminal characteristics for the various circuit elements, permits systematic analysis of any electrical network, to analyze a network or a circuit is to know the voltage across and the current in every element.

Defining a node as **"simply a point in a circuit at which two or more circuit elements join"**, Kirchhoff's current law states: **"The algebraic sum of all the currents at any node in a circuit equals zero** Mathematically, KCL can be expressed:

$$\sum_{n=1}^{N} I_n = 0 \quad \ldots\ldots\ldots\ldots (2-1)$$

A variety of statements can be found in different texts. Where I_n is the *n*th current entering (or leaving) the node and *N* is the number of node currents.

As an example consider Fig. (2-1), the nodes are labeled **a**, **b**, **c** and **d**, while the branches are numbered **1**, **2**... and **6**. At nodes a – d, the following four equations (constraints) hold.

For node **a**,

$$I_1 - I_2 - I_3 = 0$$

For node **b**,

$$I_3 + I_4 - I_5 = 0$$

For node **c**,

$$-I_1 - I_4 - I_6 = 0$$

For node **d**,

$$I_2 + I_5 + I_6 = 0$$

…….. (2-2)

In the algebraic sum (equations 2-2) we assigned a plus sign to those branch currents whose direction points into the node and vice versa. KCL is of extreme importance, and of the following features:

1- KCL imposes a linear constraint on the branch currents, equations 2-2 are linear homogeneous algebraic equations.

KCL is independent of the nature of the lumped elements, i.e. it does not matter whether the elements are, linear, non-linear, active … etc.

2- KCL expresses the conservation of charge at any and every node.

In order to state Kirchhoff's voltage law, it is necessary first to define a loop or a closed path , simply, a loop is a traversed path (two or more branches in succession) whose starting node is the same as its ending one.

Kirchhoff's voltage law states that: **"The algebraic sum of all the voltages around any closed path in a circuit equals zero"**.

Mathematically, KVL can be expressed:

$$\sum_{n=1}^{N} V_n = 0 \ldots\ldots\ldots\ldots (2-3)$$

Where V_n is the *n*th, voltage in a loop of *N* voltages.

In order to apply KVL, assign a reference direction to the loop (see Fig. 2-1, d1, d2) for the example loops chosen, all voltages in line with the reference direction, have a plus sign and vice versa. Therefore, the loop voltage equations (constraints) for the two loops chosen:

For loop **1**,

$$-V_4 - V_5 + V_6 = 0$$

For loop **2**,

$$V_1 + V_2 - V_4 - V_5 = 0$$

..... (2-4)

The followings are the features of KVL,

1- KVL imposes a linear constraint between branch voltages of a loop.

2-KVL applies to any lumped electric circuit; it does not matter whether the circuit elements are linear, non linear, passive… etc. In other wards, KVL is independent of the nature of the elements.

2.4.Procedure:

Connect the circuit shown in Fig 2-2

1- Make a record of all the branch currents with regards to their signs.
2- Make a record of all the branch voltages (with polarities).
3- Replace resistor R_3 by the filament lamp and repeat **2**, **3**.
4- Enter your data obtained in table 2-1 and verify Kirchhoff's Law's accordingly.
5- Derive the proper equations for all branch currents and voltages in terms of E_1, E_2, R_1, R_2, R_3, using KCL and KVL. (**For time saving, you can do this step before-hand at your spare time**).
6- Compare the results of 6 after substituting for the unknowns, with those obtained in **2** and **3**. Enter calculated values of current and voltage in table 2-1

2.5. Discussion

1- Derive $V_x = V \times \dfrac{R_x}{R_x + R_y}$ in the circuit shown in Fig (2-5).

2- Derive $I_x = I \times \dfrac{R_y}{R_x + R_y}$ in the circuit shown in Fig (2-6).

3- Comment on the results obtained in the practically implemented And theoretical implemented.

4- Define Kirchhoff's Laws for voltage and current.

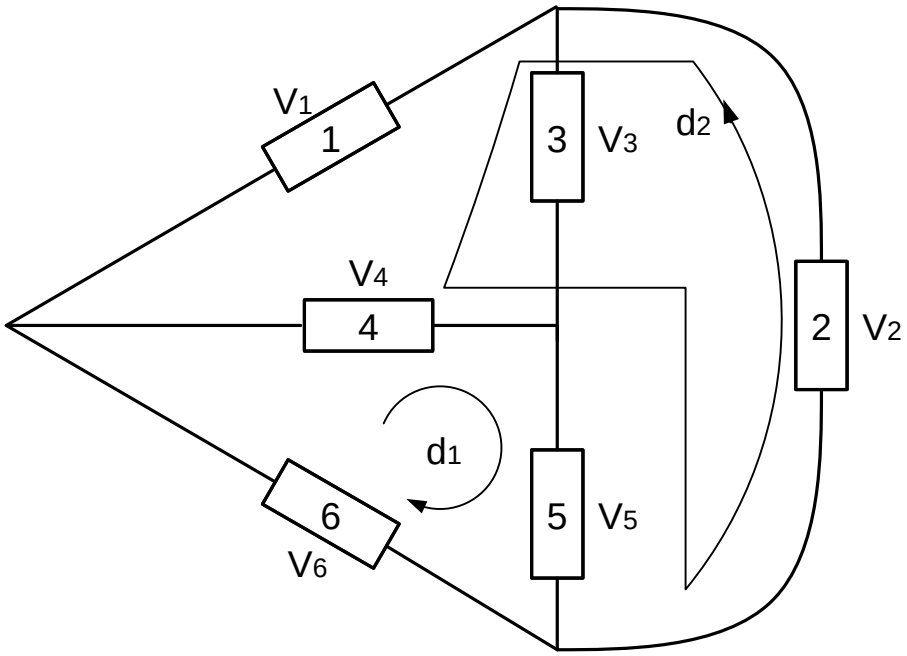

Fig (2-1)

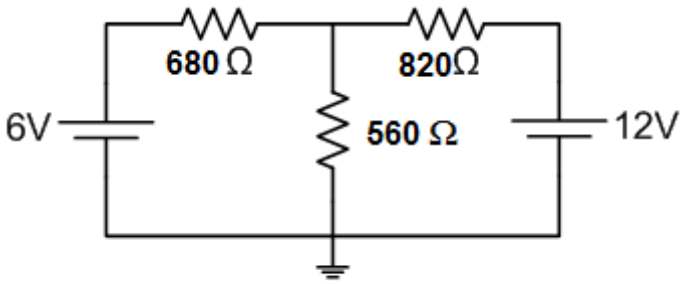

Fig (2-2)

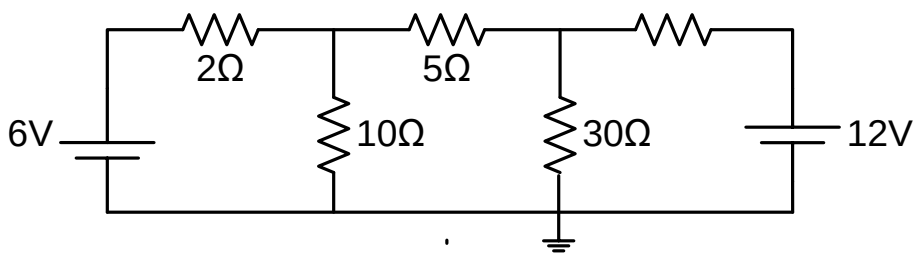

Fig (2-3)

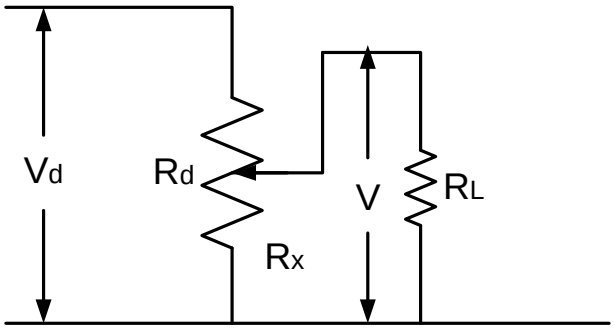

Fig (2-4)

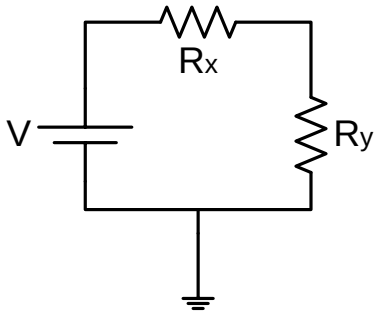

Fig (2-5)

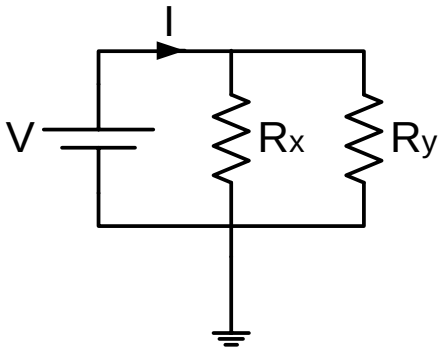

Fig (2-6)

Find of all the branch currents and voltages (with polarities) in the circuit shown in the Fig (2-7).

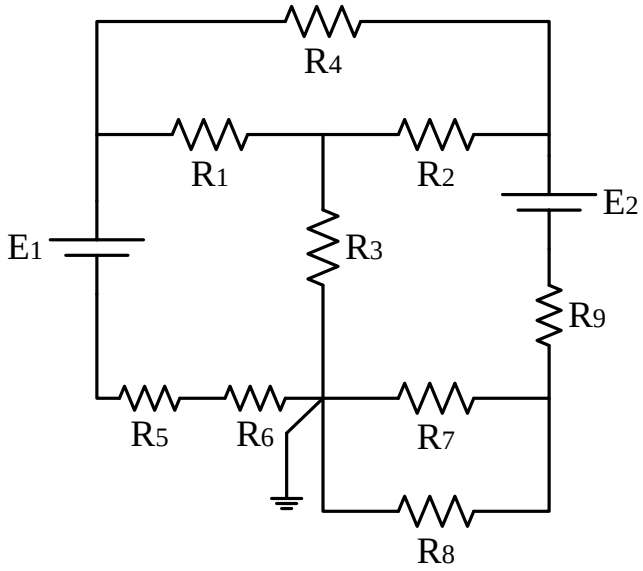

Fig (2-7)