Lecturer: Dr. Ameer Al-khaykan

Lecture: Diode Clamping Circuits

Basic Definition:

The clamping circuit (clamper) is one will "clamp" a signal to a different dc level. The circuit must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant τ = RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval (T/2) the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants. Therefore, the condition required for the capacitor to hold its voltage during the discharge period between pulses of the input signal is

$$5\tau = 5RC >> \frac{T}{2} = \frac{1}{2f}$$

In general, the following steps may be helpful when analysing clamping networks:

1. Start the analysis of clamping networks by considering that part of the in put signal that will forward bias the diode.

2. During the period that the diode is in the “on” state, assume that the capacitor will charge up instantaneously to a voltage level determined by the

network.

3. Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.

4. Throughout the analysis maintain a continual awareness of the location

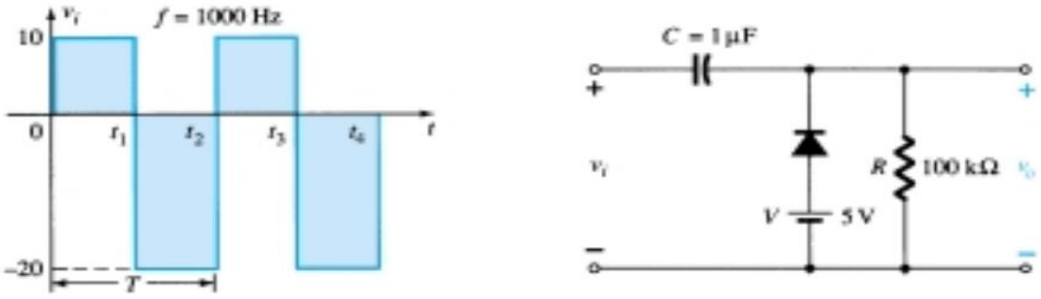
and reference polarity for vo to ensure that the proper levels for vo are obtained.

5. Keep in mind the general rule that the total swing of the total output must

match the swing of the input signal

Example

Determine v_o for the network of Fig. 2.96 for the input indicated.



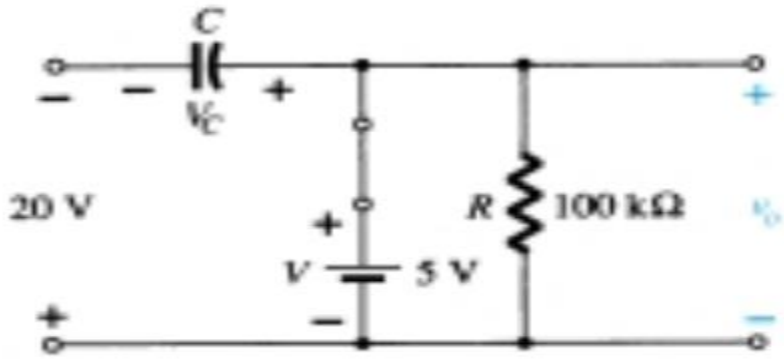
Solution

Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state as recommended by comment 1. For this interval the network will appear as shown in Fig. 2.97. The output is across R, but it is also directly across the 5-V battery if you follow the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop will result in

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$



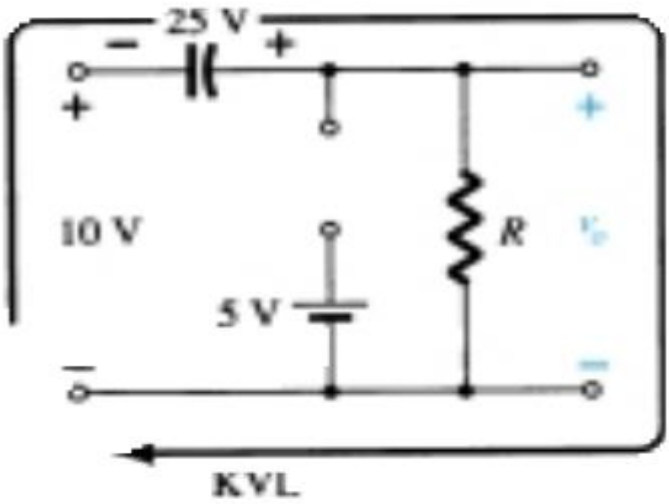
The capacitor will therefore charge up to 25 V, as stated in comment 2. In this case the resistor R is not shorted out by the diode but a Thévenin equivalent circuit of that portion of the network which includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.98.

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

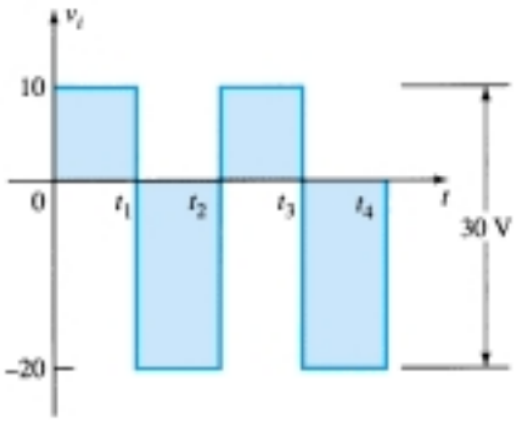


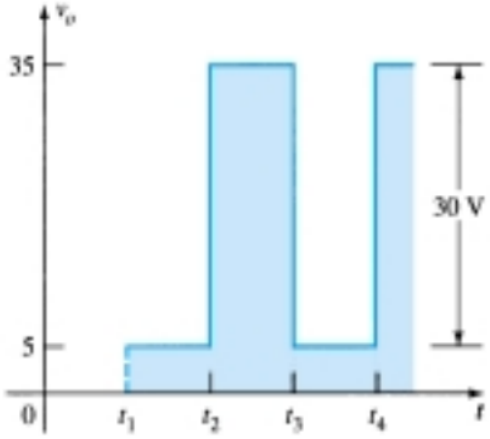
The time constant of the discharging network of Fig. 2.98 is determined by the product RC and has the magnitude

$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.99 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.





Example 4-2:

Using silicon diode, design a clamper circuit that will produce output $v_o = 10Sin\omega t - 5$ V when the input is $v_i = 10Sin\omega t + 5$ V. Draw the circuit diagram and the input and output signals.

Solution:

From the input (v_i) and output (v_o) signals, we have a negative biased clamper. Therefore, the diode is forward bias ("on" state) during the positive half period of the input signal (v_i). The output voltage (v_o) at this positive period can be determined by KVL in the output section of the circuit shown in Fig. 4-5.

$$E + 0.7 - v_o = 0 \quad => \quad E = 5 - 0.7 = 4.3 \text{ V}.$$

For the input section KVL will result in

$$15 - V_C - 5 = 0 \quad => \quad V_C = 10 \text{ V}.$$

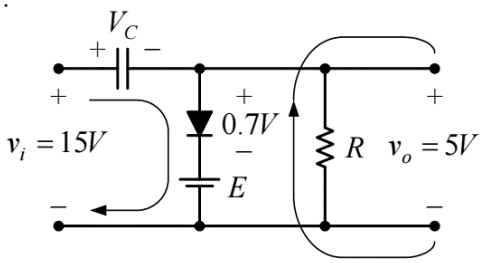
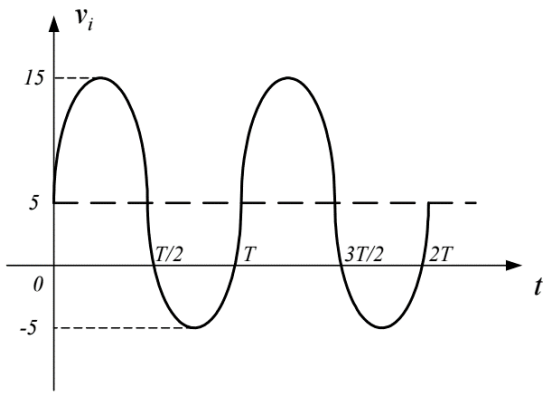
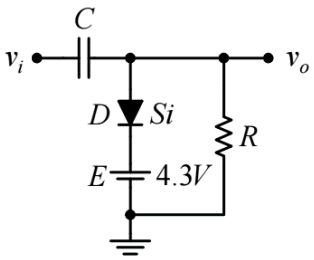
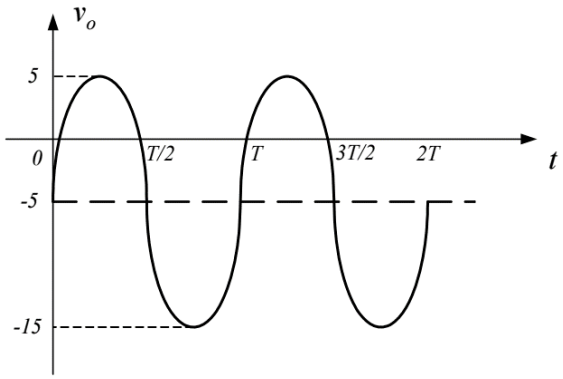


Fig. 4-5

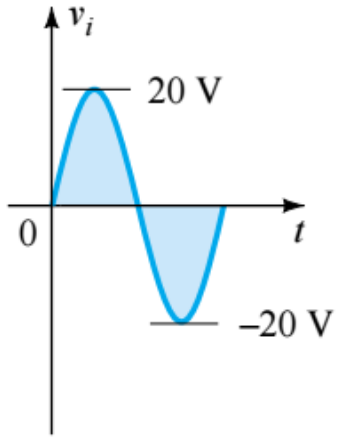
The circuit diagram and the input and output signals are shown in Fig. 4-6.

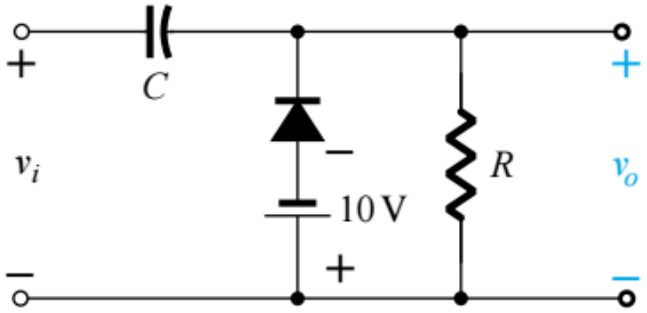


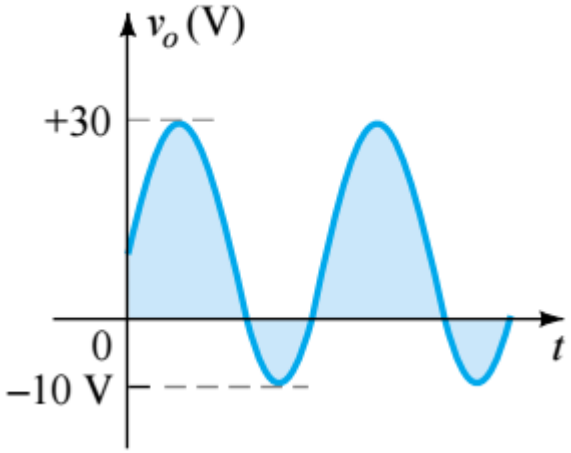




Example:

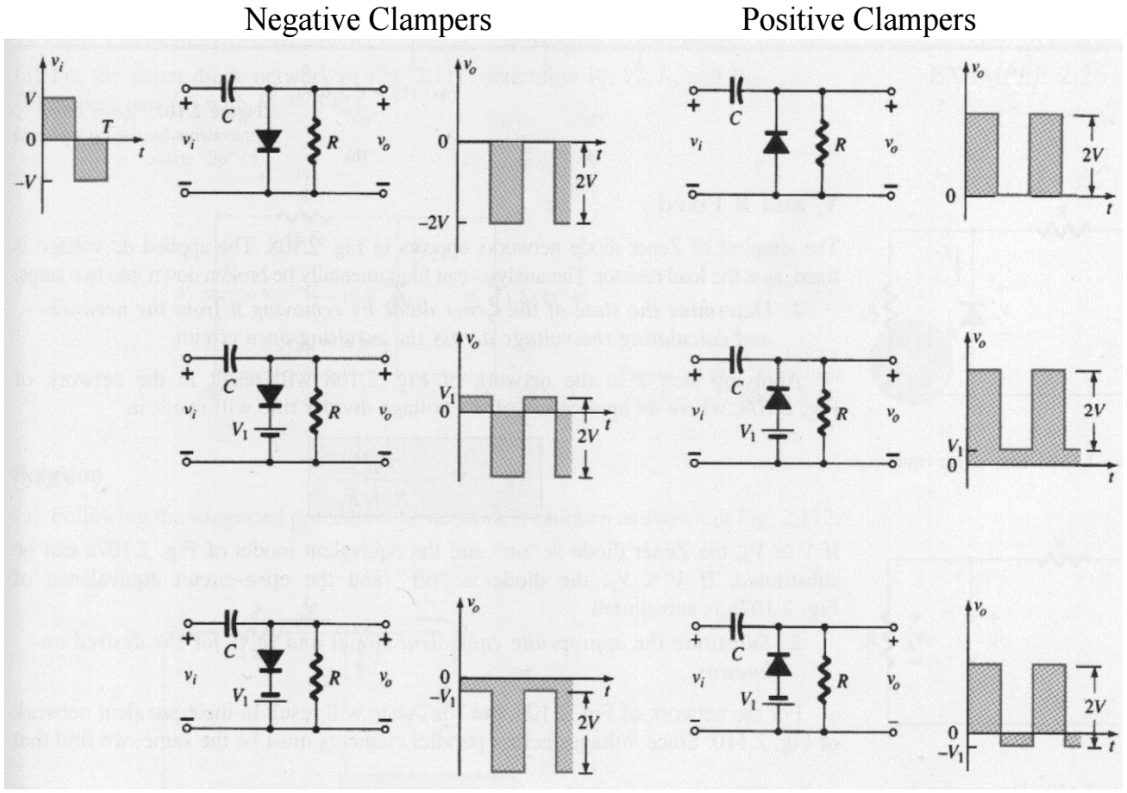






Summary:

A number of clamping circuits and their effect on the square-wave input signal are shown in Fig. 4-7.



Clampers with ideal diodes and $5\tau = 5RC >> T/2$

Fig. 4-7

Exercise:

Sketch the output (v_o) for the circuit of Fig. 4-8 for the input (v_i) shown. Assume ideal diodes.