AL MUSTAQBAL UNIVERSITY COLLEGE

STUDENT NAME:	
TUTOR NAME:	**Dr. Ameer Al-khaykan**
PROGRAMME:	**Electrical Circuit**
SUBJECT:	**Electrical and Electronics**
COURSEWORK TITLE:	**Clamper Circuit Diode**

Issue Date:	**Due Date:**	**Feedback Date:**	**Extension Date:**

PERFORMANCE CRITERIA:

TARGETED LEARNING OUTCOMES

4. Solve problems involving basic analogue and digital electronic circuits using numerical skills appropriate to an engineer.

5. Identify and safely use standard laboratory equipment to extract data, then apply in the solution of an electronic or electrical engineering problem;

6. Adopt a logical approach to the solution of engineering problems.

Important Information – Please Read Before Completing Your Work

All students should submit their work by the date specified using the procedures specified in the Student Handbook. An assessment that has been handed in after this deadline will be marked initially as if it had been handed in on time, but the Board of Examiners will normally apply a lateness penalty.

Your attention is drawn to the Section on Academic Misconduct in the Student's Handbook.

All work will be considered as individual unless collaboration is specifically requested, in which case this should be explicitly acknowledged by the student within their submitted material.

Any queries that you may have on the requirements of this assessment should be e-mailed to **ameer.alkhaykan@mustaqbal-college.edu.iq**
No queries will be answered after respective submission dates.
You must ensure you retain a copy of your completed work prior to submission.

MARKING CRITERIA

COURSEWORK WILL BE MARKED ACCORDING TO THE FOLLOWING UNIVERSITY CRITERIA.

90-100%: a range of marks consistent with a first where the work is exceptional in all areas;

80-89%: a range of marks consistent with a first where the work is exceptional in most areas.

70-79%: a range of marks consistent with a first. Work which shows excellent content, organisation and presentation, reasoning and originality; evidence of independent reading and thinking and a clear and authoritative grasp of theoretical positions; ability to sustain an argument, to think analytically and/or critically and to synthesise material effectively.

60-69%: a range of marks consistent with an upper second. Well-organised and lucid coverage of the main points in an answer; intelligent interpretation and confident use of evidence, examples and references; clear evidence of critical judgement in selecting, ordering and analysing content; demonstrates some ability to synthesise material and to construct responses, which reveal insight and may offer some originality.

50-59%: a range of marks consistent with lower second; shows a grasp of the main issues and uses relevant materials in a generally business-like approach, restricted evidence of additional reading; possible unevenness in structure of answers and failure to understand the more subtle points: some critical analysis and a modest degree of insight should be present.

40-49%: a range of marks which is consistent with third class; demonstrates limited understanding with no enrichment of the basic course material presented in classes; superficial lines of argument and muddled presentation; little or no attempt to relate issues to a broader framework; lower end of the range equates to a minimum falls short in one or more areas.
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35-39%: achieves many of the learning outcomes required for a mark of 40% but falls short in one or more areas.

30-34%: a fail; may achieve some learning outcomes but falls short in most areas; shows considerable lack of understanding of basic course material and little evidence of research.

0-29%: a fail; basic factual errors of considerable magnitude showing little understanding of basic course material; falls substantially short of the learning outcomes for compensation.

Note:

- While constructing circuits all connects should be made with the power supply in the off position.
- Check power and ground connections (and other connections) **before** switch on the power.
- Make sure that the power and the ground are properly connected to all IC's before switch on the power.
- **DO NOT** strip wire ends longer than 1/4" and jam long bare ends into the breadboard holes. This will cause shorts and ruin the board.
- **DO NOT** short (connect) the power supply outputs together, i.e., do not allow the exposed wires to touch each other. This will cause permanent damage to the power supply.
- **DO NOT** connect the power supply to the breadboard with reverse polarity. This will cause the permanent chip damage.

- **DO NOT** connect an output of any gate to the output of another gate, to a switch, to power (+5V), or to ground. These situations will cause excessive currents and result in the permanent damage to the chip or chips involved.

4.1 Objects:

1. To know the connection of the clamper circuits, and to know the response of each circuit on the Oscilloscope.
2. To know the application of each circuit.
3. To Show how the output voltage has change when compared to the input voltage waveforms.

4.2 Theory:

In some practical situations we might need to make wave-shaping to the AC input signal by adding a DC level to the input waveform, this special type of wave shaping circuits is called the diode clampers. This type of wave-shaping circuits doesn't change the input signal shape. In this experiment, we are going to construct these circuits and to watch its output signal practically.

Clamping means that there is a part of the circuit will clip out and added to the other part. This process uses the capacitor to generate these circuits. There is one condition for this circuit that the time constant of the capacitor charging and discharging must be the period time of the wave by 5 (5RC>T).

There are two types of the clamper circuits: the positive clamper as shown in figure (1) and the negative clamper as shown in figure (3).

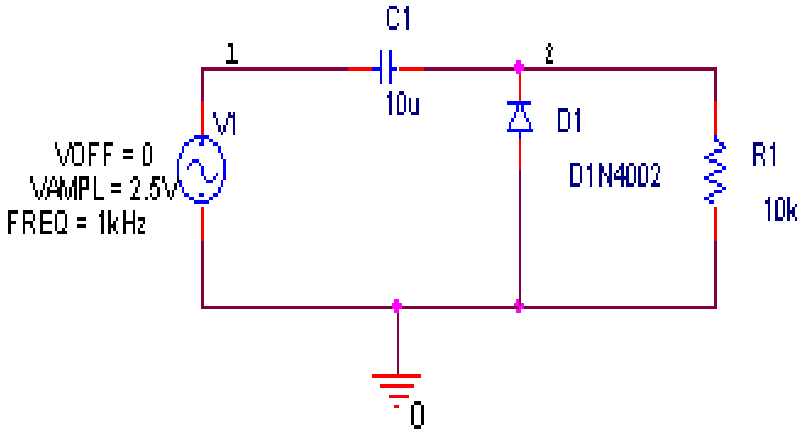

Figure (1): The positive Clamper Circuit

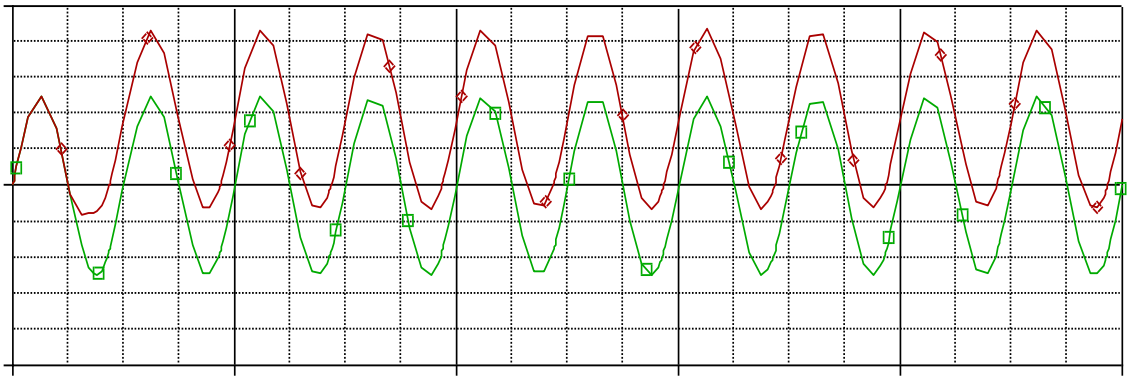

Figure (2): The input and the output voltages to the positive clamper circuit

Figure (1) shows the diagram of the positive clampers, because the output signal is above the input one, in the following steps, we are going to build the negative clamper by only reversing the diode polarity.

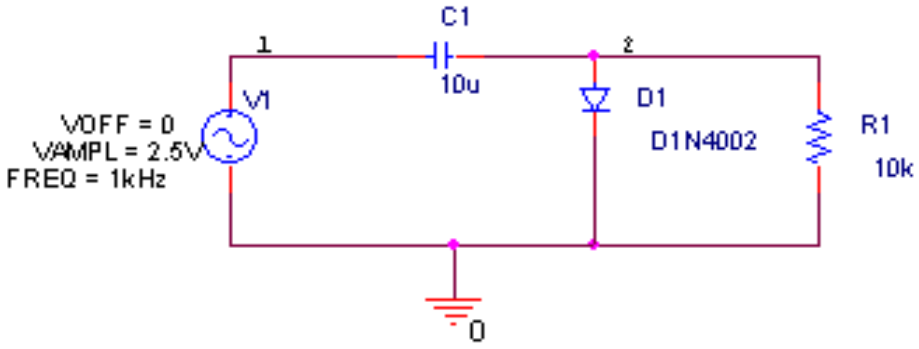

Figure (3): The Negative Clamper Circuit

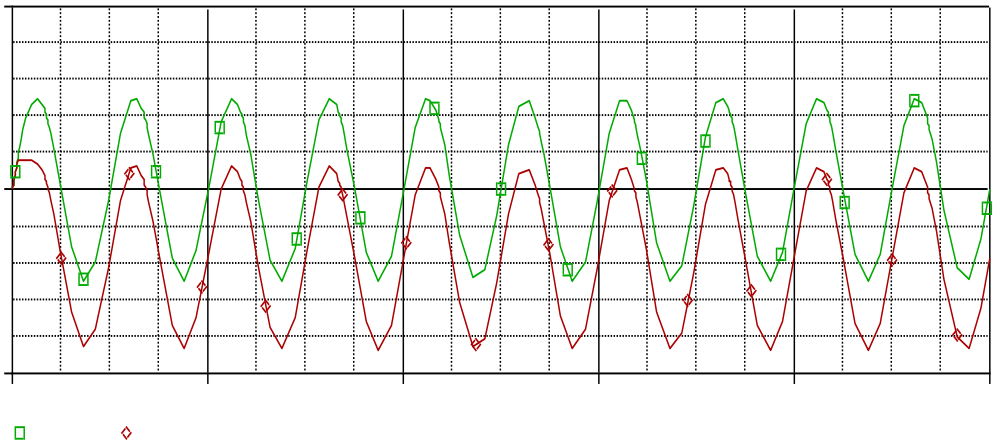

Figure (4): The input and the output voltages to the negative clamper circuit

You must note in both the positive and negative diode clamper circuit that the clamped curves doesn't locate at the zero axis but above or below it by the barrier potential of the diode in the forward bias status of the diode, because in the forward bias status of the diode, the diode maintains prescribed amount of voltage called the barrier potential.

4.3 Equipments:

1. Function generator.
2. 15k ohm resistor.
3. 1N4001 silicon rectifier diode.
4. Oscilloscope.
5. DC power supply.

4.4 Procedure:

1) Positive clamper circuit:

1. Connect the clamper circuit shown in figure (1).
2. Adjust the signal generator to 5 V (P-P) and choose the frequency of the signal (1 kHz) in this circuit.
3. Connect the oscilloscope to the output terminal of the circuit in figure (1) (at the terminal of the load resistor) and measure the output voltage.
4. Switch on the signal generator and draw the input and output signal curves as shown in figure (2).

2) Negative clamper circuit:

1. Connect the clamper circuit shown in figure (3).

2. Adjust the signal generator to 5 V (P-P) and choose the frequency of the signal (1 kHz) in this circuit.

3. Connect the oscilloscope to the output terminal of the circuit in figure (3) (at the terminal of the load resistor) and measure the output voltage.

4. Switch on the signal generator and draw the input and output signal curves as shown in figure (4).

4.5Discussion

1. Why the capacitor is used in the clamper circuits?

2. Give some uses of the clamper circuits.

3. Compare between the clipper and the clamper circuits.

4.6 Review Questions

1. For the circuit of figure(1) to function properly, the input frequency should be at least
   (a) 1 Hz (b) 10 Hz (c) 100 Hz (d) 1 kHz

2. For the circuit of figure (3), if the input signal has a peak voltage of VP, then the output signal is

   (a) Shifted upward by approximately VP

   (b) Shifted upward by approximately 2VP

   (c) Shifted downward by approximately VP

   (d) Shifted downward by approximately 2VP

3. For the circuit of figure (1), the negative peak voltage of the output signal is approximately

   (a) –VP (b) −0.7 V (c) 0 V (d) +0.7V

4. If the peak to peak input voltage is increased,

   (a) The peak to peak output voltage remains approximately equal to the peak to peak input voltage

   (b) The negative peak output voltage remains clamped at approximately -0.7V

   (c) The output peak voltage approximately equals the peak-to-peak input voltage

   (d) all of the above

5. In order to change the circuit of figure (1) to a negative clamper, you must

(a) Reverse the polarity of the signal source

(b) Reverse the polarity of the diode

(c) Reverse the polarity of the capacitor

(d) all of the above