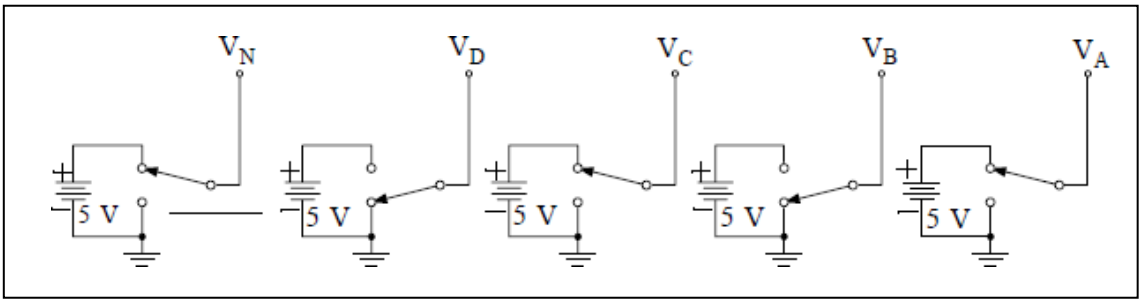
Digital to Analog (DAC) AND Analog to Digital (ADC) Converters

Electric voltage and current signals are often referred to as analog signals. Analog signals must be converted to digital signals prior to input into computers. Analog to Digital Converters (ADCs) are used to convert analog signals to digital signals. Inversely, the computer output that is in digital form must sometimes be converted to analog signal prior to input to an electrical device. Digital to Analog Converters (DACs) are used to perform this operation. In this chapter we will examine the important characteristics associated with ADC/DAC converters.

- **Digital-to-Analog Converters:**

  Digital systems recognize only two levels of voltage referred to as HIGH and LOW signals or as logical 1 and logical 0. This two-level scheme works well with the binary numbers system. It is customary to indicate the HIGH (logical 1) and LOW (logical 0) by Single-Pole-Double-Throw (SPDT) switches that can be set to a positive non-zero voltage like 5 volts for HIGH and zero volts or ground for LOW as shown in figure below.



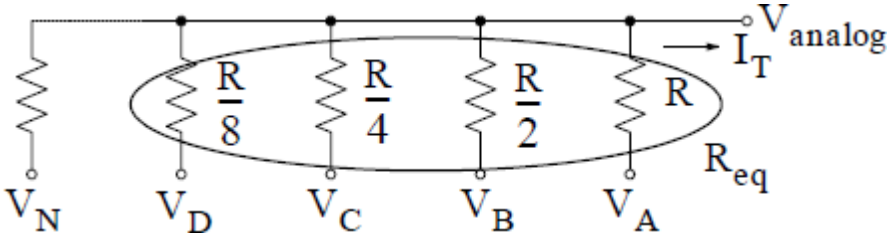
In the above figure, $V_D = 0$, $V_C = 1$, $V_B = 0$ and $V_A = 1$, that is, switches A and C are HIGH (5 volts) and switches B and D are LOW (0 volts).

The first 16 binary numbers representing all possible combinations of the four switches with voltage settings V_A (least significant position) through V_D (most significant position) and their decimal equivalents are shown in table below:

Voltage Level				Binary Equivalent				Decimal Equivalent
V_D	V_C	V_B	V_A	A	B	C	D	
LOW	LOW	LOW	LOW	0	0	0	0	0
LOW	LOW	LOW	HIGH	0	0	0	1	1
LOW	LOW	HIGH	LOW	0	0	1	0	2
LOW	LOW	HIGH	HIGH	0	0	1	1	3
LOW	HIGH	LOW	LOW	0	1	0	0	4
LOW	HIGH	LOW	HIGH	0	1	0	1	5
LOW	HIGH	HIGH	LOW	0	1	1	0	6
LOW	HIGH	HIGH	HIGH	0	1	1	1	7
HIGH	LOW	LOW	LOW	1	0	0	0	8
HIGH	LOW	LOW	HIGH	1	0	0	1	9
HIGH	LOW	HIGH	LOW	1	0	1	0	10
HIGH	LOW	HIGH	HIGH	1	0	1	1	11
HIGH	HIGH	LOW	LOW	1	1	0	0	12
HIGH	HIGH	LOW	HIGH	1	1	0	1	13
HIGH	HIGH	HIGH	LOW	1	1	1	0	14
HIGH	HIGH	HIGH	HIGH	1	1	1	1	15

A digital to analog (DAC) converter is used to convert a binary output from a digital system to an equivalent analog voltage. If there are 16 combinations of the voltages V_D through V_A, the analog device should have 16 possible values. For example, since the binary number 1010 (decimal 10) is twice the value of the binary number 0101 (decimal 5), an analog equivalent voltage of 1010 must be double the analog voltage representing 0101.

- **DAC (Binary-Weighted Resistors):**



Digital-to-Analog converter using binary-weighted resistors

$$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D + \ldots.}{1 + 2 + 4 + 8 + \cdots..}$$

Prove:

$$I_T = I_A + I_B + I_C + I_D$$

$$I_T = \frac{V_A}{R} + \frac{V_B}{R/2} + \frac{V_C}{R/4} + \frac{V_D}{R/8}$$

$$I_T = \frac{1}{R}\,(V_A + 2V_B + 4V_C + 8V_D)$$

Using parallel resistor law:

$$\frac{1}{R_{eq}} = \frac{1}{R} + \frac{1}{R/2} + \frac{1}{R/4} + \frac{1}{R/8}$$

OR:

$$R_{eq} = \frac{R}{1 + 2 + 4 + 8}$$

Since:

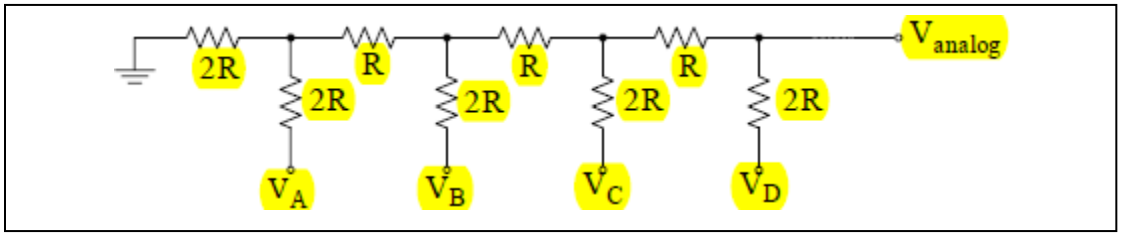
$$V_{analog} = R_{eq}\, I_T$$

$$V_{analog} = \frac{R}{1+2+4+8} * \frac{1}{R}\,(V_A + 2V_B + 4V_C + 8V_D)$$

$$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{1 + 2 + 4 + 8}$$

The binary-weighted resistors shown in figure above have the disadvantage that it requires a large number of precision resistors.

- **R-2R ladder network:**



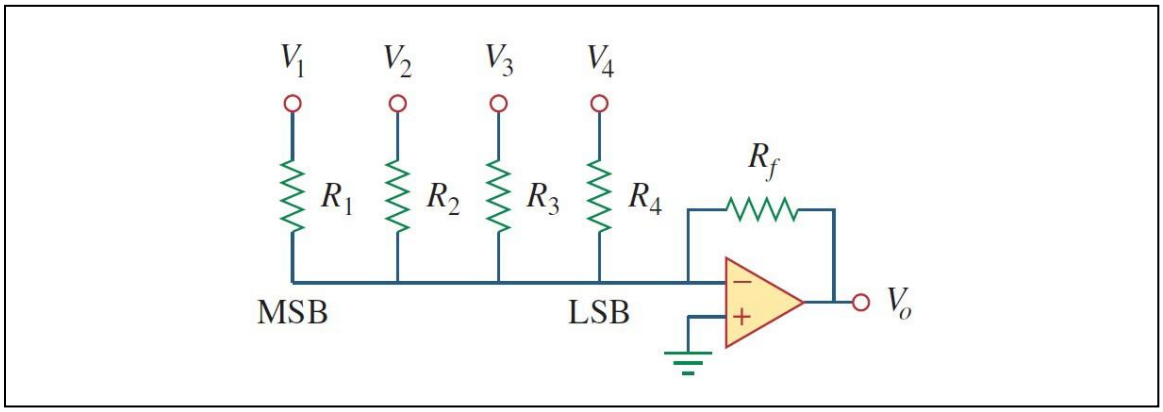
The above figure show R-2R ladder network. It requires more resistors, but only two sets of precision resistance values, R and 2R. The output analog voltage V_{analog} of the above figure can be obtained from the relation.

$$\boldsymbol{V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n}}$$

Where n is the number of digital inputs.

The problem with the DAC covered so far is that if one loads its output (draw current from its output) the circuit will be unbalance. The loading causes the circuit's output voltage to change, and the circuit will no longer accurately convert our digital to a proportional analog signal. To prevent loading the DAC, it is good idea to add a unity-gain buffer to the output of the DAC.

A typical example of four-bit DAC is illustrated in figure below; the four-bit can be realized using the binary weighted resistors shown in figure below. The bits are weighted according to the magnitude of their place value, so that lesser bit has half the weight of the next higher bit. The output (analog) related to the input (digital) shown in the following equation.



$$-V_o = \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 + \frac{R_f}{R_4} V_4$$

The above figure shows a DAC connected to an inverting amplifier; alternatively, a non-inverting op amp could be used with a positive value of V_{ref}.

Example 1: For the DAC circuit in the above figure, Given: R_f = 10 K, R_1 = 10 K, R_2 = 20 KΩ, R_3 = 40 KΩ, R_4 = 80 KΩ and $V_{ref} = 1$ V.

Find the analog output voltage for the following digital input [0000],[0001],[0010],……, [1111].

Solution:

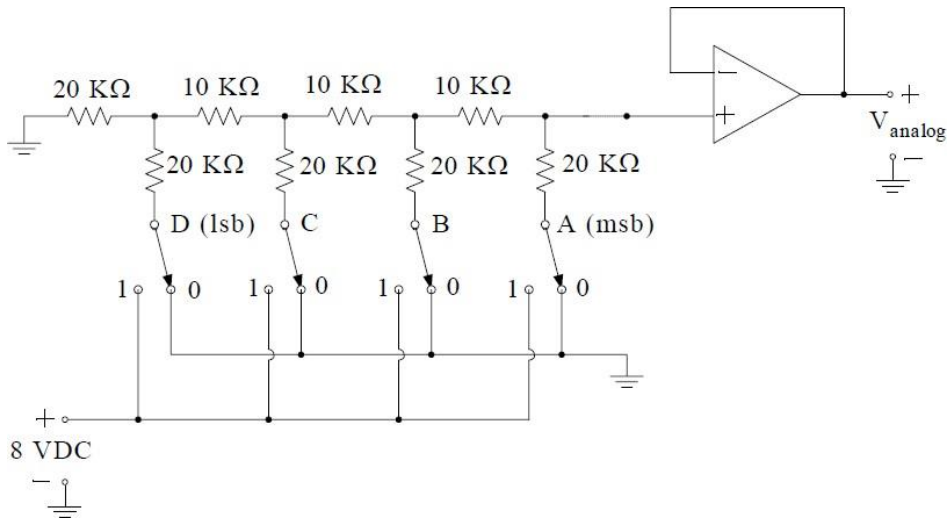
$$-\boldsymbol{V_o} = \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 + \frac{R_f}{R_4} V_4$$

$$-\boldsymbol{V_o} = \frac{10}{10} V_1 + \frac{10}{20} V_2 + \frac{10}{40} V_3 + \frac{10}{80} V_4$$

$$-\boldsymbol{V_o} = V_1 + 0.5\, V_2 + 0.25\, V_3 + 0.125\, V_4$$

Binary input $[V_1V_2V_3V_4]$	Decimal value	Output $-V_o$
0000	0	0
0001	1	0.125
0010	2	0.25
0011	3	0.375
0100	4	0.5
0101	5	0.625
0110	6	0.75
0111	7	0.875
1000	8	1.0
1001	9	1.125
1010	10	1.25
1011	11	1.375
1100	12	1.5
1101	13	1.625
1110	14	1.75
1111	15	1.875

Example 2: Given the R-2R DAC circuit in figure below, find the output for the digital input signal in the following table.



Input Digital Signals:

	A 2^0	B 2^1	C 2^2	D 2^3	
(a)	1	1	1	1	
(b)	1	0	0	1	
(c)	1	0	1	0	
(d)	0	1	0	0	

Solution:

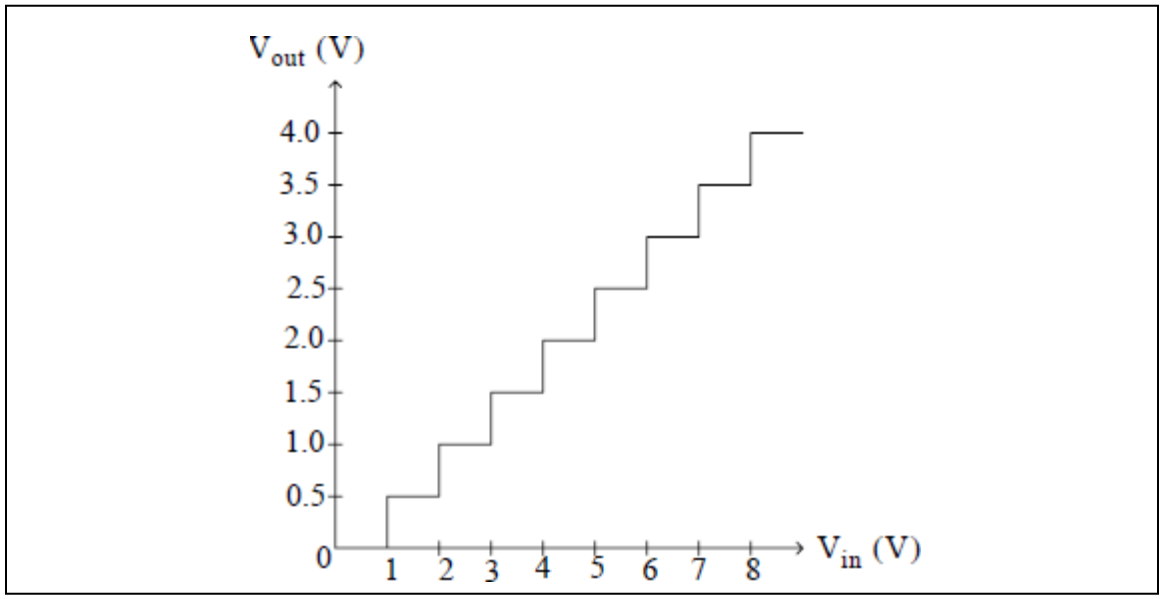
$$a)\ V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1*8 + 2*8 + 4*8 + 8*8}{2^4} = \mathbf{7.5\ V}$$

$$b)\ V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1*8 + 2*0 + 4*0 + 8*8}{2^4} = \mathbf{4.5\ V}$$

$$c)\ V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1*8 + 2*0 + 4*8 + 8*0}{2^4} = \mathbf{2.5\ V}$$

$$d)\ V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1*0 + 2*8 + 4*0 + 8*0}{2^4} = \mathbf{1.0\ V}$$

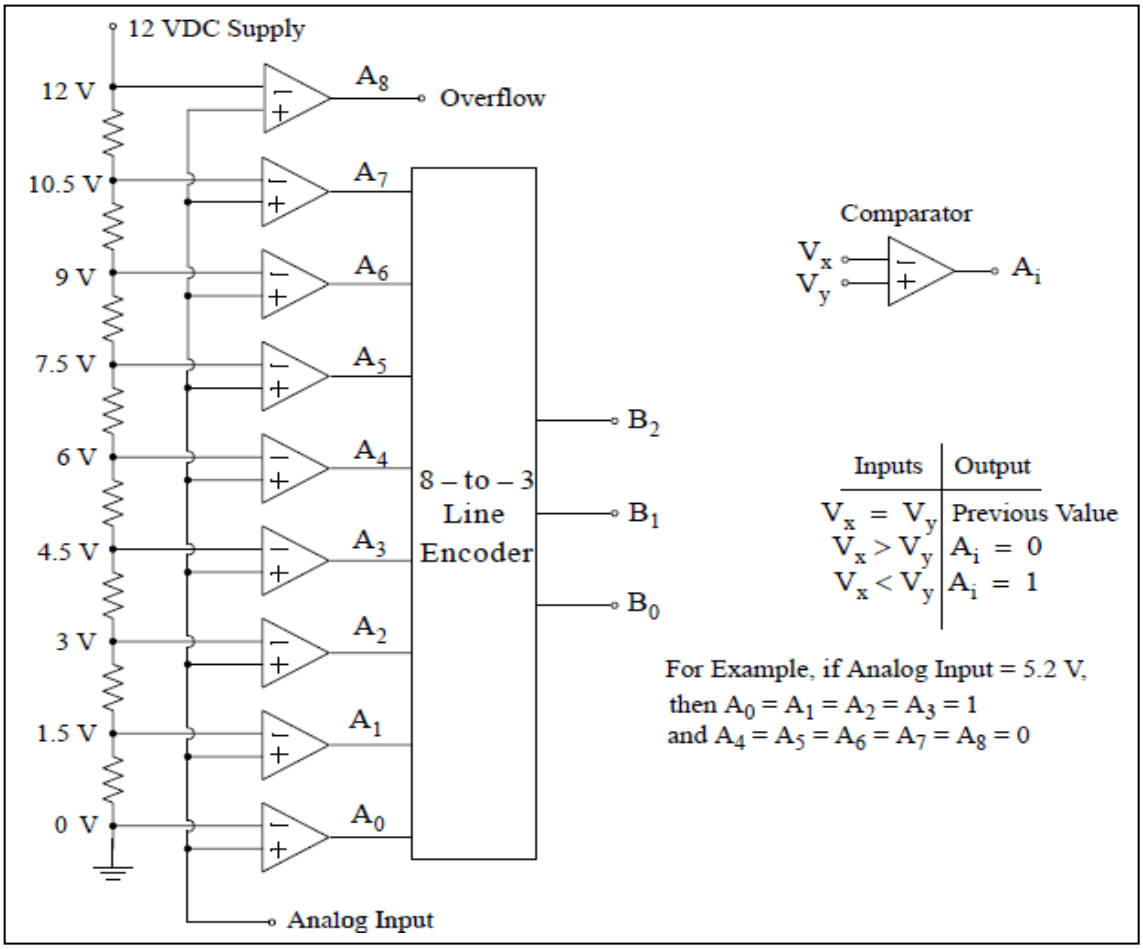
Based on these results, we can plot the output versus the inputs voltages of the R-2R network.



Analog to Digital (ADC)
Converters

Often an analog voltage must be converted to a digital equivalent, such as in a digital voltmeter. In such cases, the principle of the previously discussed digital-to-analog or D/a converter or simply DAC can be reversed to perform analog-to-digital A/D conversion. There are different types of analog-to-digital converters, usually referred to as ADC, such as:

1. **The Flash Analog-to-Digital (Parallel) Converter:** Figure below shows a typical flash type ADC consists of a resistive network, comparators, and 8-to-3 line encoder. The flash ADC is so named because of its high conversion speed.



Rules

Inverting > non-inverting = 0

Inverting < non-inverting = 1

Inverting = non-inverting = previous value

Components

Voltage Divider

Comparator

Priority Encoder

Truth Table for 8-to-3 line encoder

Analog Input	A8	A7	A6	A5	A4	A3	A2	A1	A0	B2	B1	B0
Less than 0 V	0	0	0	0	0	0	0	0	0	x	x	x†
0 to less than 1.5 V	0	0	0	0	0	0	0	0	1	0	0	0
1.5 to less than 3.0 V	0	0	0	0	0	0	0	1	1	0	0	1
3.0 to less than 4.5 V	0	0	0	0	0	0	1	1	1	0	1	0
4.5 to less than 6.0 V	0	0	0	0	0	1	1	1	1	0	1	1
6.0 to less than 7.5 V	0	0	0	0	1	1	1	1	1	1	0	0
7.5 to less than 9.0 V	0	0	0	1	1	1	1	1	1	1	0	1
9.0 to less than 10.5 V	0	0	1	1	1	1	1	1	1	1	1	0
10.5 to 12 V	0	1	1	1	1	1	1	1	1	1	1	1
Greater than 12 V	1	1	1	1	1	1	1	1	1	x	x	x‡
† Underflow												
‡ Overflow												

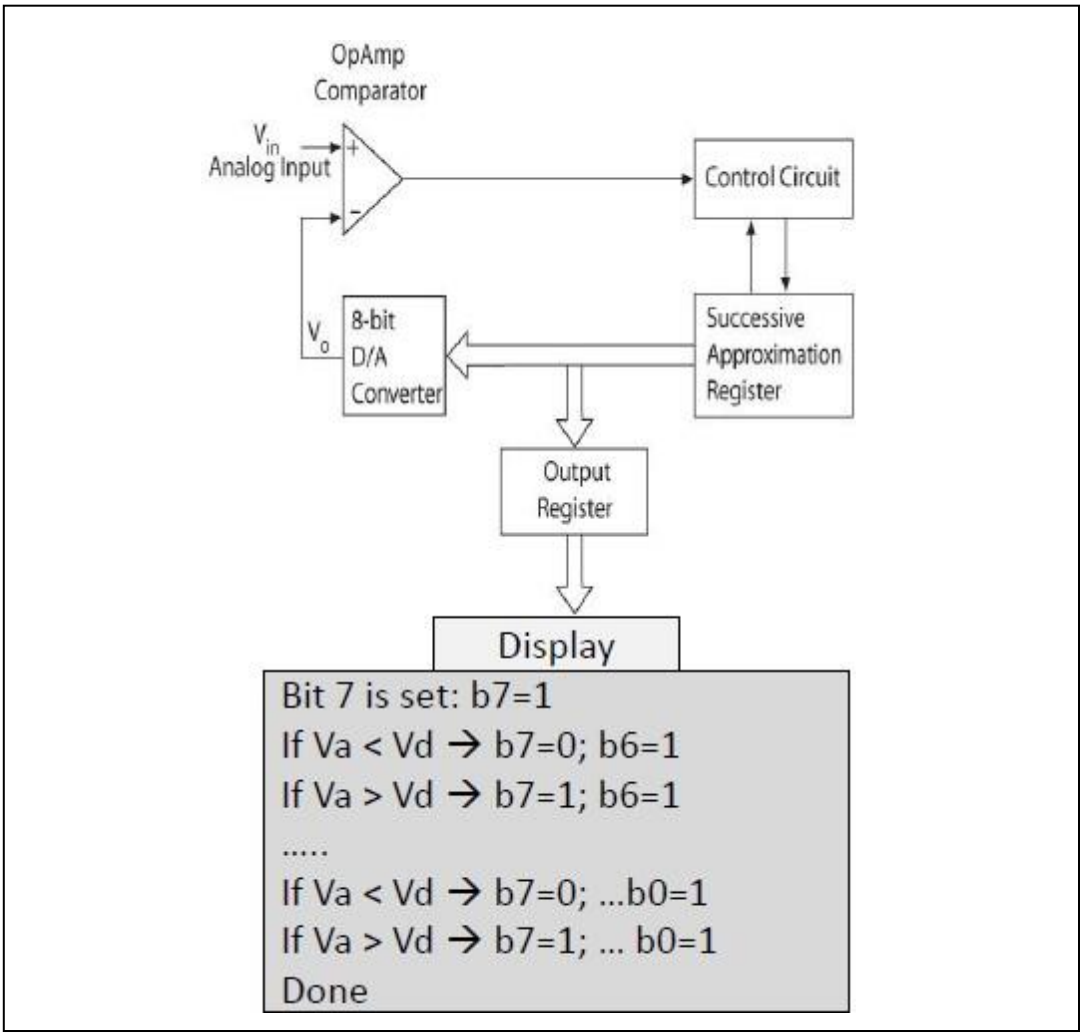
Example (1): Using Flash Analog to Digital Converter circuit in figure below and the following input V_{ref} (12 Volt) , V_{analog} (5.5 Volt), Find the digital output.

Output is: (011)

Example (2): Using Flash Analog to Digital Converter circuit in figure below and the following input V_{ref} (8 Volt) , V_{analog} (3.5 Volt), Find the digital output.

Example (3): Using Flash Analog to Digital Converter circuit in figure below and the following input V_{ref} (8 Volt) , V_{analog} (5.5 Volt), Find the digital output.

2. **Successive approximation converter:** figure below shows a typical successive approximation type ADC.



- The SAR (successive approximation register) begins by turning on the MSB (Bit 7).
- V_o of the D/A converter is compared with the analog input voltage V_{in} in the comparator.
- If analog input voltage is less than the digital voltage, Bit 7 is turned off and Bit 6 is turned on.
- If analog input voltage is greater than the digital voltage, Bit 7 is kept on and Bit 6 is turned on.
- The process of turning bit on/off is continued until bit 0.

- Now the 8-bit input to the D/A converter represents the digital equivalent of the analog signal V_{in}.

Example: using the 8-bit successive approximation converter (ADC), fined thebinary output for analog input voltage V_{an} = 0.049 volt.

Solution:

V_{analog} = 0.049 volt X 1000 = 49 mv

For 8-bit ADC start with the set high the MSB 10000000

1	0	0	0	0	0	0	0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
128	64	32	16	8	4	2	1

Van=49 ≥ 128	10000000	NO	$= 0$
Van ≥ 64	01000000	NO	$= 0$
Van ≥ 32	00100000	yes	$= 1$
Van ≥ 32 + 16	00110000	yes	$= 1$
Van ≥ 32 + 16 + 8	00111000	NO	$= 0$
Van ≥ 32 + 16 + 4	00110100	NO	$= 0$
Van ≥ 32 + 16 + 2	00110010	NO	$= 0$
Van ≥ 32 + 16 + 1	00110001	yes	$= 1$

Total binary output = 00110001